



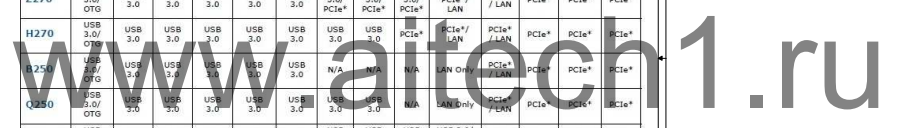
# B25H4-AM

Rev:1.0

**ECS**  
**CONFIDENTIAL**

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SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Z270	USB 3.0/OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0/PCIe*	USB 3.0/PCIe*	USB 3.0/PCIe*	USB 3.0/PCIe*/LAN	PCIe*/LAN	PCIe*	PCIe*	PCIe*
H270	USB 3.0/OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	PCIe*	PCIe*/LAN	PCIe*/LAN	PCIe*	PCIe*	PCIe*
B250	USB 3.0/OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	None	None	None	LAN Only	PCIe*/LAN	PCIe*	PCIe*	PCIe*
Q260	USB 3.0/OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	M.2	USB 3.0 only	PCIe*/LAN	PCIe*	PCIe*	PCIe*
Q270	USB 3.0/OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0/PCIe*	USB 3.0/PCIe*	USB 3.0/PCIe*	USB 3.0/PCIe*/LAN	PCIe*	PCIe*	PCIe*	PCIe*

SKU	15 <sup>1</sup>	16 <sup>1</sup>	17	18	19 <sup>1</sup>	20 <sup>1</sup>	21	22	23	24	25	26
<b>Z770</b> (See Note 1)	PC1e <sup>+</sup> / LAN / SATA1a	PC1e <sup>+</sup> / SATA1a	PC1e <sup>+</sup>	PC1e <sup>+</sup> / LAN	PC1e <sup>+</sup> / LAN / SATA0a	PC1e <sup>+</sup> / SATA1b	PC1e <sup>+</sup> / SATA2	PC1e <sup>+</sup> / SATA3	PC1e <sup>+</sup> / SATA4	PC1e <sup>+</sup> / SATA5	PC1e <sup>+</sup>	PC1e <sup>+</sup>
<b>H270</b> (See Note 2)	PC1e <sup>+</sup> / LAN / SATA0a	PC1e <sup>+</sup> / SATA1a	PC1e <sup>+</sup>	PC1e <sup>+</sup> / LAN	PC1e <sup>+</sup> / LAN / SATA0a	PC1e <sup>+</sup> / SATA1b	PC1e <sup>+</sup> / SATA2	PC1e <sup>+</sup> / SATA3	SATA4	SATA5	PC1e <sup>+</sup>	PC1e <sup>+</sup>
<b>B250</b>	PC1e <sup>+</sup> / LAN / SATA0a	PC1e <sup>+</sup> / SATA1a	PC1e <sup>+</sup>	PC1e <sup>+</sup> / LAN	SATA0b	SATA1b	SATA2	SATA3	SATA4	SATA5	N/A	N/A
<b>Q250</b>	PC1e <sup>+</sup> / LAN / SATA0a	PC1e <sup>+</sup> / SATA1a	PC1e <sup>+</sup>	PC1e <sup>+</sup> / LAN	PC1e <sup>+</sup> / LAN / SATA0b	PC1e <sup>+</sup> / SATA1b	SATA2	SATA3	SATA4	SATA5	N/A	N/A
<b>Q270</b> (See Note 2)	PC1e <sup>+</sup> / LAN / SATA0a	PC1e <sup>+</sup> / SATA1a	PC1e <sup>+</sup>	PC1e <sup>+</sup> / LAN	PC1e <sup>+</sup> / LAN / SATA0b	PC1e <sup>+</sup> / SATA1b	PC1e <sup>+</sup> / SATA2	PC1e <sup>+</sup> / SATA3	PC1e <sup>+</sup> / SATA4	PC1e <sup>+</sup> / SATA5	PC1e <sup>+</sup>	PC1e <sup>+</sup>

- Table 1-5. PCH-H HSIO Detail (Lane 27-30)

SKU	27	28	29	30
<b>Z270</b> (see Note 2)	PC1e*	PC1e*	PC1e*	PC1e*
<b>H270</b> (see Note 2)	PC1e*	PC1e*	PC1e*	PC1e*
<b>B25</b> (see Note 2)	PC1e*	PC1e*	PC1e*	PC1e*
<b>Q250</b> (see Note 2)	PC1e*	PC1e*	PC1e*	PC1e*
<b>Q270</b> (see Note 2)	PC1e*	PC1e*	PC1e*	PC1e*

 Elitegroup Computer Systems

## PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPP_D7	3VSB	GPP_D7_CASEOPEN (reserved)	GPIO(GPI)
GPP_D6	3VSB	GPP_D6_BIOSWP	GPIO(GPI)
GPP_D5	3VSB	GPP_D5_BIOS_WP	GPIO(GPI)
GPD10	ATX_3VSB	GPD10 (ME disable by SW)	SLP_S5#
GPD2	ATX_3VSB	ILAN_WAKE_L	LAN_WAKE#
GPD0	ATX_3VSB	RLAN_PWR_EN (only for B25 sku)	BATLOW#
GPD11	ATX_3VSB	LAN_DIS_L	LANPHYPC
GPP_A12	3VSB	GPP_A12_TPM H:with on-board TPM L:W/O on-board TPM	GPIO(GPI)
GPP_G16	3VSB	LPC_PME_L	GPIO(GPI)
GPP_G13	VCC3	HDPANEL_DETECT (reserved)	GPIO(GPI)
GPP_A14	VCC3	LPCPD_L	SUS_STAT#
GPP_A0	VCC3	KBRST_L_RC	RCIN#
GPP_A6	VCC3	SERIRQ	SERIRQ
GPP_A5	N/A	LPC_FRAME_L	LFRAME#
GPP_A1	N/A	LPC_LAD0	LAD0
GPP_A2	N/A	LPC_LAD1	LAD1
GPP_A3	N/A	LPC_LAD2	LAD2
GPP_A4	N/A	LPC_LAD3	LAD3
GPP_A9	N/A	PCH_SIO_24M	CLKOUT_LPC0
GPP_A10	N/A	TCM_TPM_24M	CLKOUT_LPC1
GPP_B3	VCC3	BT_DISABLE_L L:disable	GPIO(GPI)
GPP_B17	VCC3	WLAN_DISABLE_L L:disable	GPIO(GPI)
GPP_E8	VCC3	SATALED_L	SATA_LED#
GPP_F16	3VSB	GPP_F16 H: USB power enable	GPIO(GPI)
GPP_I0	N/A	DDPB_HPD0	DDPB_HPD0
GPP_I1	N/A	DDPC_HPD1	DDPC_HPD1
GPP_I2	N/A	DDPD_HPD2	DDPD_HPD2
GPP_I2	N/A	DDPE_HPD3	DDPE_HPD3
GPP_G23	3VSB	GPP_G22 H:default BIOS L:on-board VGA	GPIO(GPI)
GPP_F22	VCC3	GPP_F22_PCIEIRST (PCIEx16 SW RST#)	GPIO(GPI)
GPD9	ATX_3VSB	PCH_RI_L L:RI# wake up	SLP_WLAN#
GPP_H0	3VSB	ILAN_CLKREQ	SRCLKREQ0#
GPP_B6	3VSB	M2CLK_REQ1_L	SRCLKREQ1#
GPP_E0	3VSB	GPP_E0_OBR (ACER's OBR)	GPIO(GPI)
GPP_H14	3VSB	GPP_H14 (ACER reserved GPIO)	GPIO(GPI)
GPP_H15	3VSB	GPP_H15 (ACER reserved GPIO)	GPIO(GPI)
GPP_A11	3VSB	PME_L	PME#
GPP_B7	3VSB	PEX4X_REQ2_L	SRCLKREQ2#
GPP_D0	DIMM_5VDUAL	SIO_LED0	GPIO(GPI)
GPP_D1	DIMM_5VDUAL	SIO_LED1	GPIO(GPI)

## ECIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP33	3VSB	Wake up by Monitor(DP1)	SUSACK(DOD8)
GP34	3VSB	Wake up by Monitor(DP2)	SUWARN#(DI)
GP35	3VSB	Wake up by Monitor(VGA)	FAN_TAC4(DI)
GP36	3VSB	Wake up by Monitor(HDMI)	FAN_CTL3(DOD8)
GP37	ATX_5VSB	DP Wake up by Monitor control	FAN_TAC3(DI)
RI2# GP17	3VSB	VGA/HDMI Wake up by Monitor control	RI2#(DI)
GP16	3VSB	basic health function	5VSB_CTRL#(DOD8)
GP31	3VSB	sleep mode wake up	PWNOUT(DOD8)
GP41	3VSB	GPP_E7_THERM	PWROK2(DOD8)

## PCH\_CPU-Strap

Pin Name	Usage	Default Status
CFG0	CFG[0]: Stall reset sequence after PCU Pin lock until de-asserted	1 = (Default) Normal Operation
CFG1	CFG[1]: Reserved configuration lane	
CFG2:5:6	CFG[2]:1 = Normal operation CFG[6:5]:11 = 1 x16 PCI Express	PCIEL6X
CFG3	CFG[3]: Reserved configuration lane.	
CFG4	CFG[4]: eDP enable:	0 = Enable
CFG7	CFG[7]: PEG Training:	1 = (default) PEG Train Immediately following RESET# de assertion.
CFG19:8	CFG[19:8]:Reserved configuration lanes.	
SPKR/GPP_B14	Top Swap Override	0 =Disable "Top Swap" mode. (Default)
GSPI0_MOSI/GPP_B18	No Reboot	0 =Disable "No Reboot" mode
SMBALERT#/GPP_C2	TIS Confidentiality	1 =EnableIntel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SMB (On-chip Security Address) with TLS
GSPI1_MOSI/GPP_B22	Hot BIOS Strap-At USB	0=SPI
SML0ALERT#/GPP_C5	eSPI or LPC	0 =LPCIs selected for EC.
HDA_SDO	Flash Descriptor Security Override	This signal has a weak internal pull-down. 0 =Enable security measures defined in the Flash Descriptor. 1 =Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
DDPB_CTRLDATA/GPP_I6	Display Port B Detected	1 = Port B is detected.
DDPC_CTRLDATA/GPP_I8	Display Port C Detected	1 = Port C is detected.
DDPB_CTRLDATA/GPP_I10	Display Port D Detected	1 = Port D is detected.

## Interrupt mapping

Function	INT#port	PCIe*1 port	Device
ILAN	INTB#	Port4	WG1219LM
RLAN	INTB#	Port6	RTL8111EPV
SATA	INTA#	NA	SATA3.0



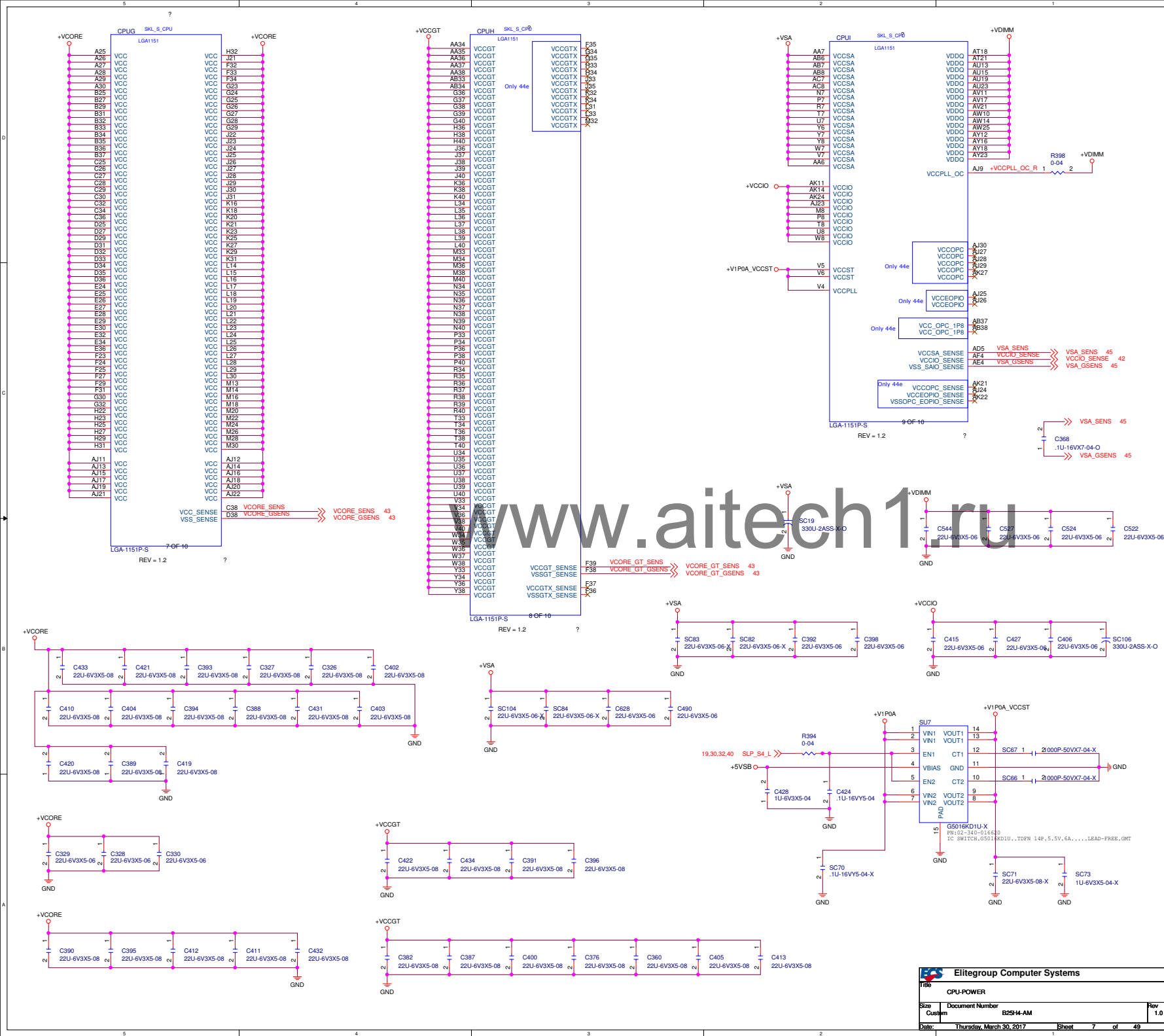


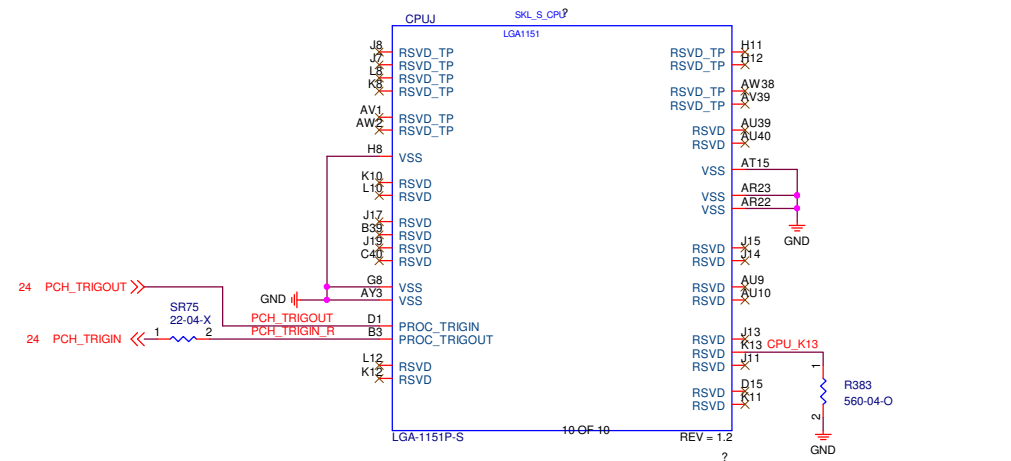
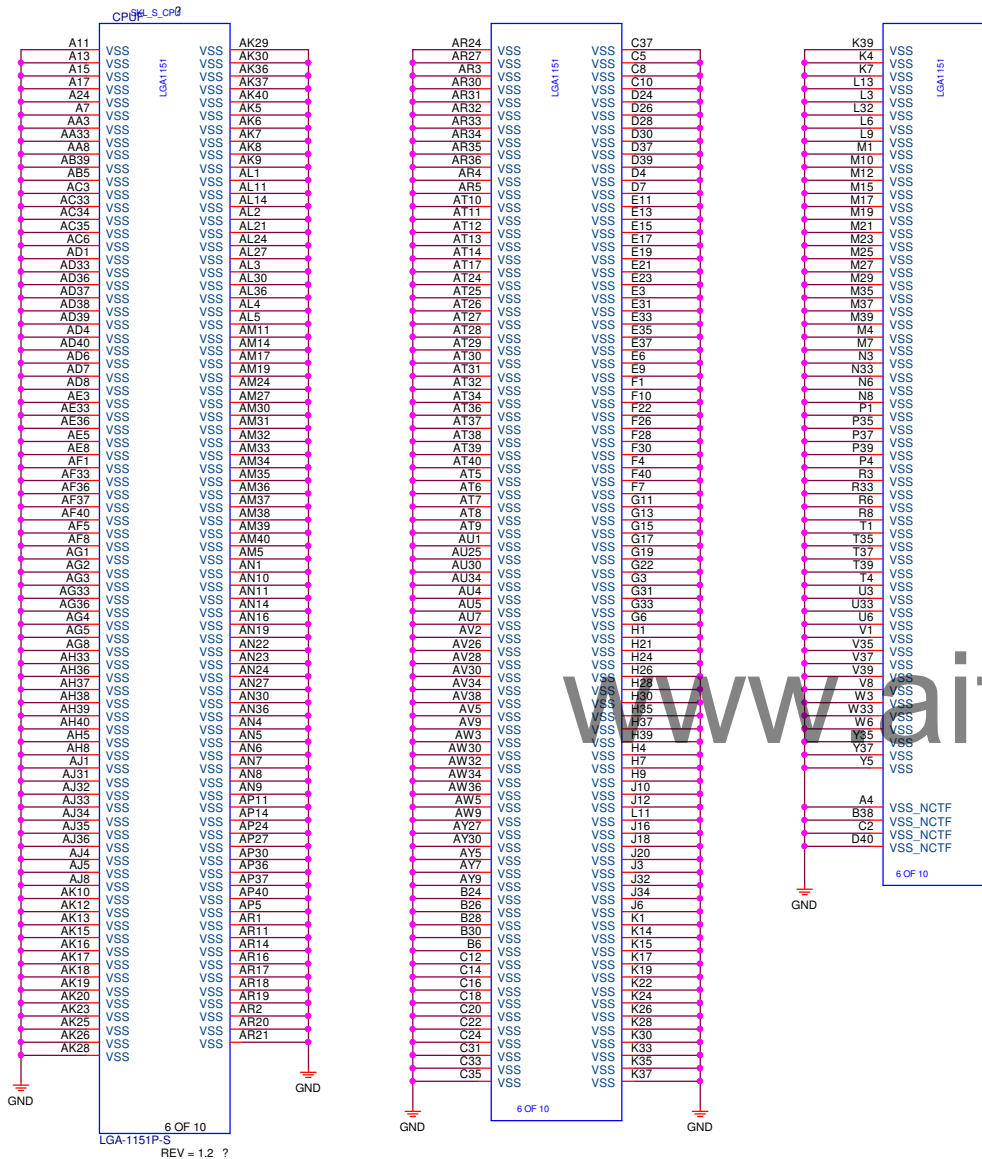


9	M_DATA_A[0..63]	《	M_DATA_A[0..63]
9	M_CLK_A_P[0..3]	《	M_CLK_A_P[0..3]
9	M_CLK_A_N[0..3]	《	M_CLK_A_N[0..3]
9	M_CKE_A[0..3]	《	M_CKE_A[0..3]
9	M_CS_A_L[0..3]	《	M_CS_A_L[0..3]
9	M_ODT_A[0..3]	《	M_ODT_A[0..3]
9	M_MA_A[0..15]	《	M_MA_A[0..15]
9	M_DQS_A_P[0..7]	《	M_DQS_A_P[0..7]
9	M_DQS_A_N[0..7]	《	M_DQS_A_N[0..7]

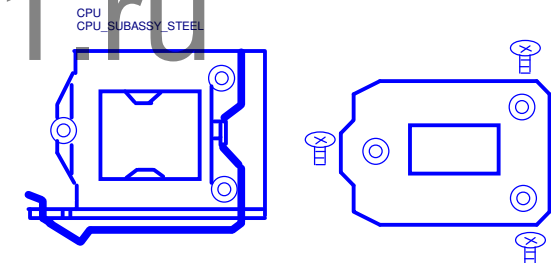
10	M_DATA_B[0..63]	《	M_DATA_B[0..63]
10	M_CLK_B_P[0..3]	《	M_CLK_B_P[0..3]
10	M_CLK_B_N[0..3]	《	M_CLK_B_N[0..3]
10	M_CKE_B[0..3]	《	M_CKE_B[0..3]
10	M_CS_B_L[0..3]	《	M_CS_B_L[0..3]
10	M_ODT_B[0..3]	《	M_ODT_B[0..3]
10	M_MA_B[0..15]	《	M_MA_B[0..15]
10	M_DQS_B_P[0..7]	《	M_DQS_B_P[0..7]
10	M_DQS_B_N[0..7]	《	M_DQS_B_N[0..7]



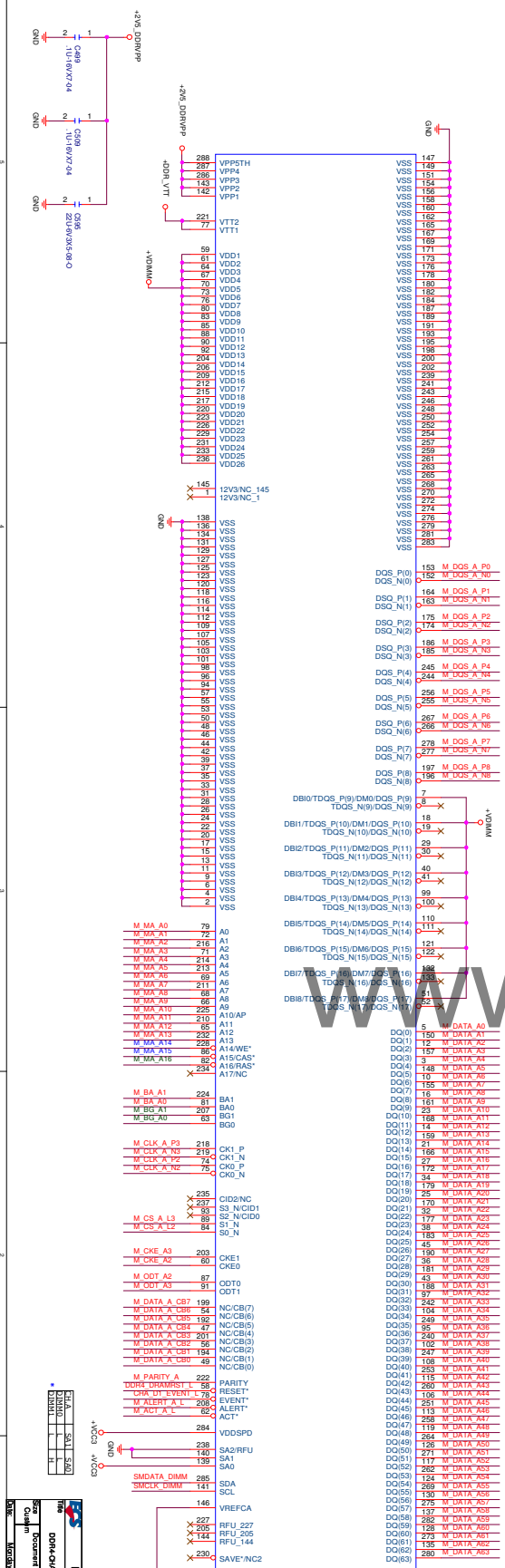
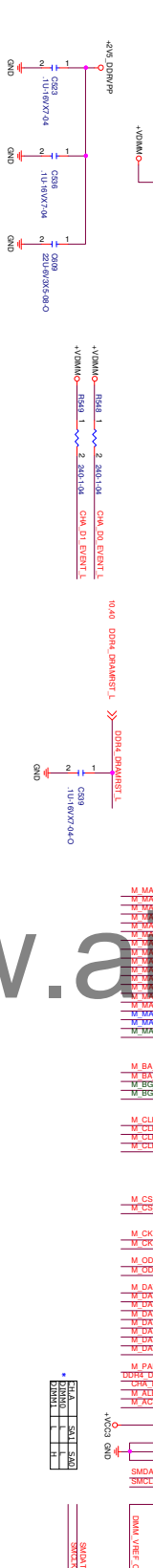
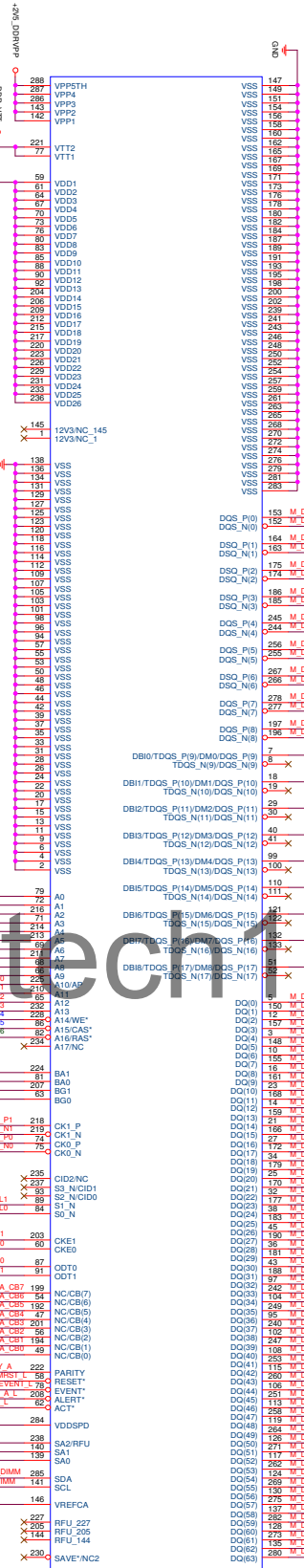
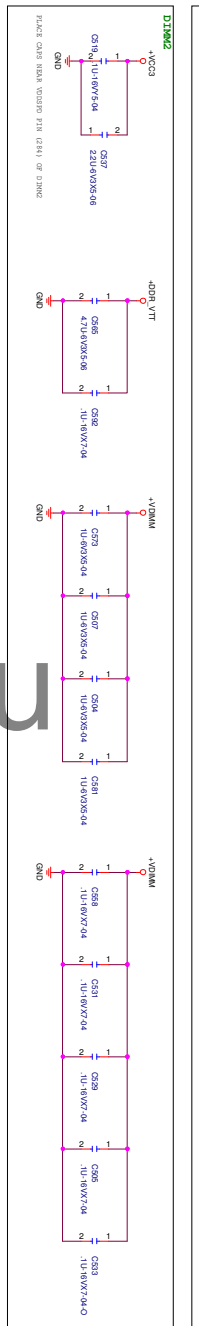
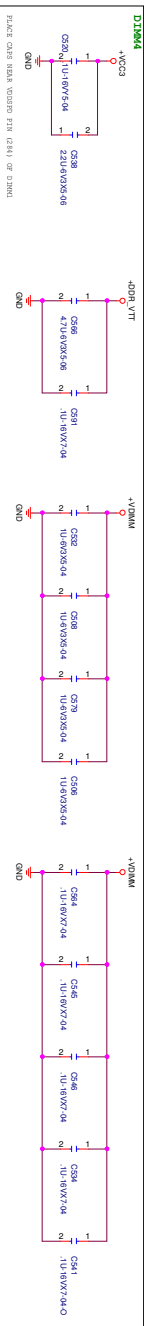
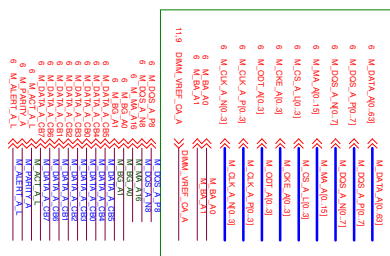




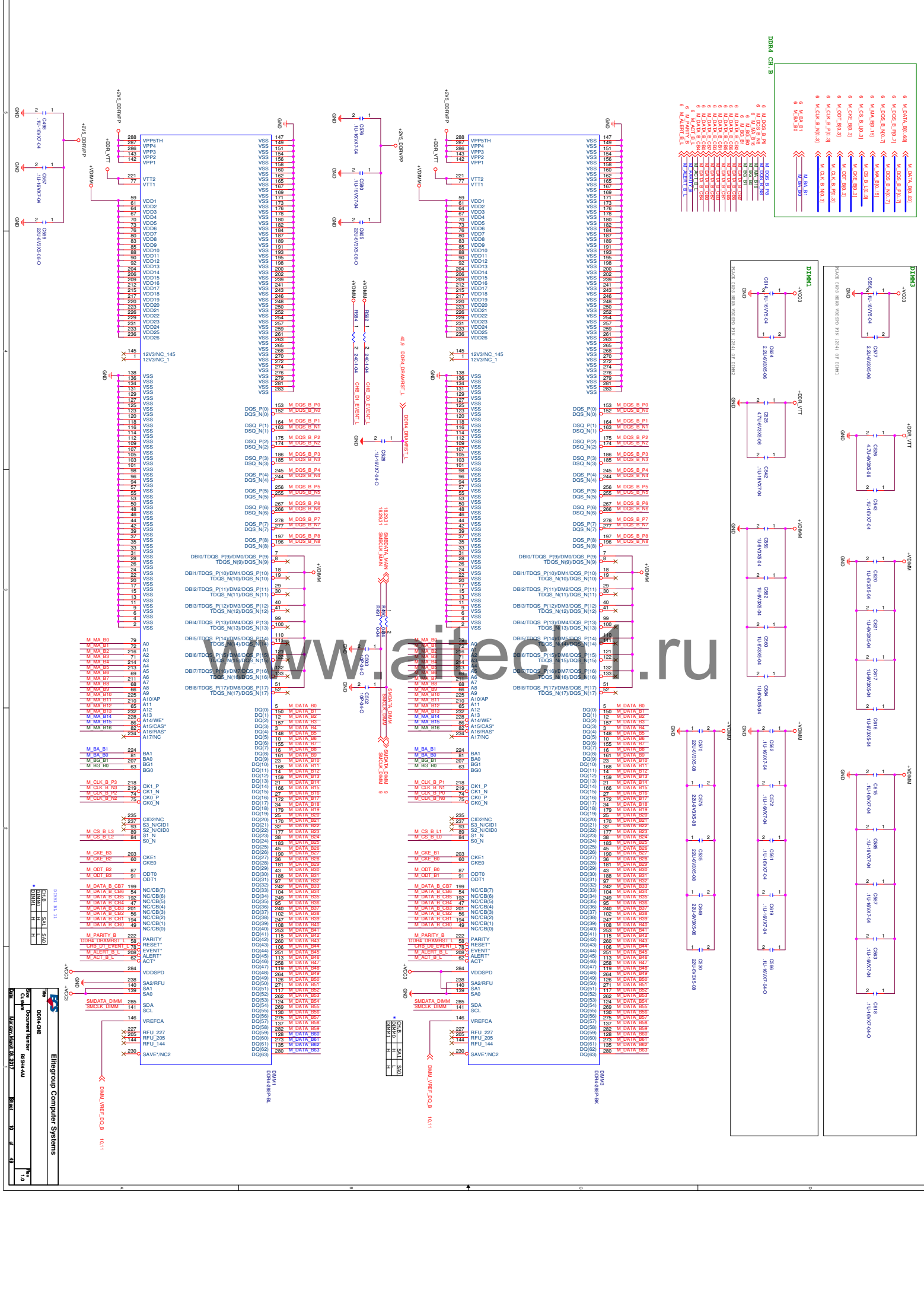
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CPU Steel (T/U phase)  
P/N:20-800-005911 SUBASSY.STEEL....LGA 1155/1156P.W/BACK PLATE.....  
ACA-ZIF-082-P38....LEAD-FREE(RoHS/HF).LOTES



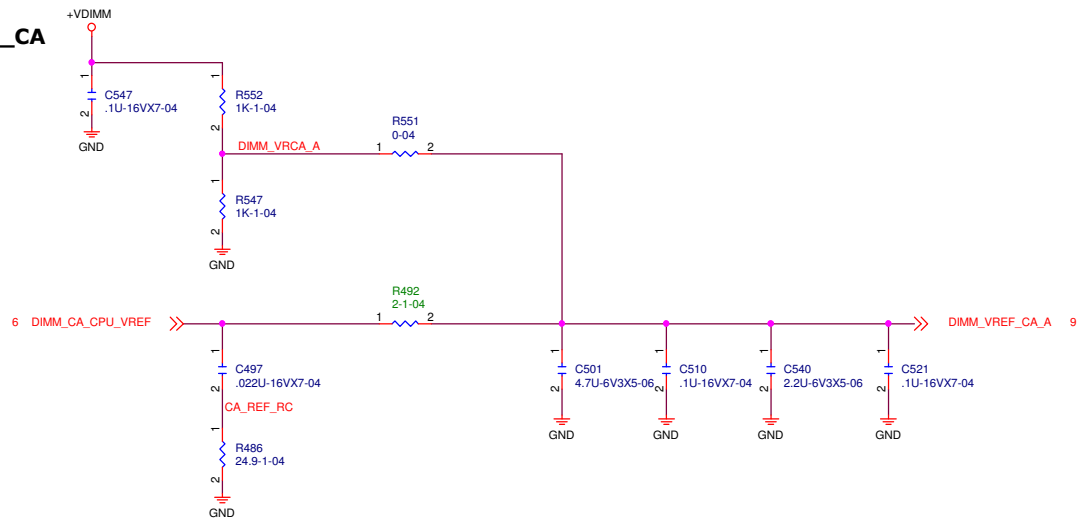




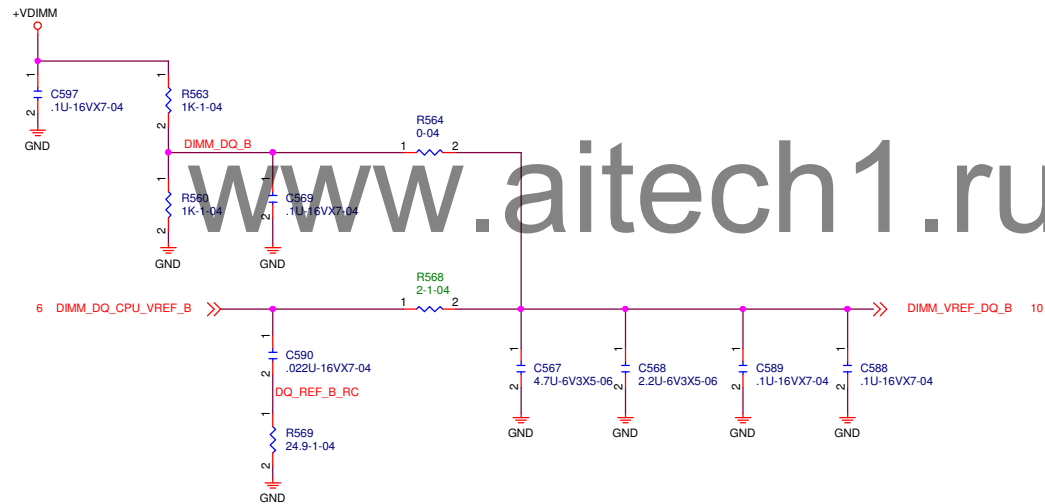
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2	U2	1	Intel Z490	Intel	
3	U3	1	Intel Z490	Intel	
4	U4	1	Intel Z490	Intel	
5	U5	1	Intel Z490	Intel	
6	U6	1	Intel Z490	Intel	
7	U7	1	Intel Z490	Intel	
8	U8	1	Intel Z490	Intel	
9	U9	1	Intel Z490	Intel	
10	U10	1	Intel Z490	Intel	
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12	U12	1	Intel Z490	Intel	
13	U13	1	Intel Z490	Intel	
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# DIMM\_VREF\_CA



# DIMM\_VREF\_DQ

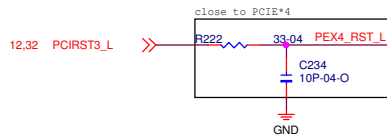




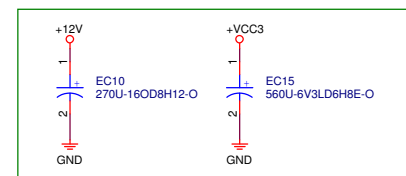
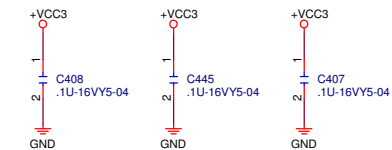
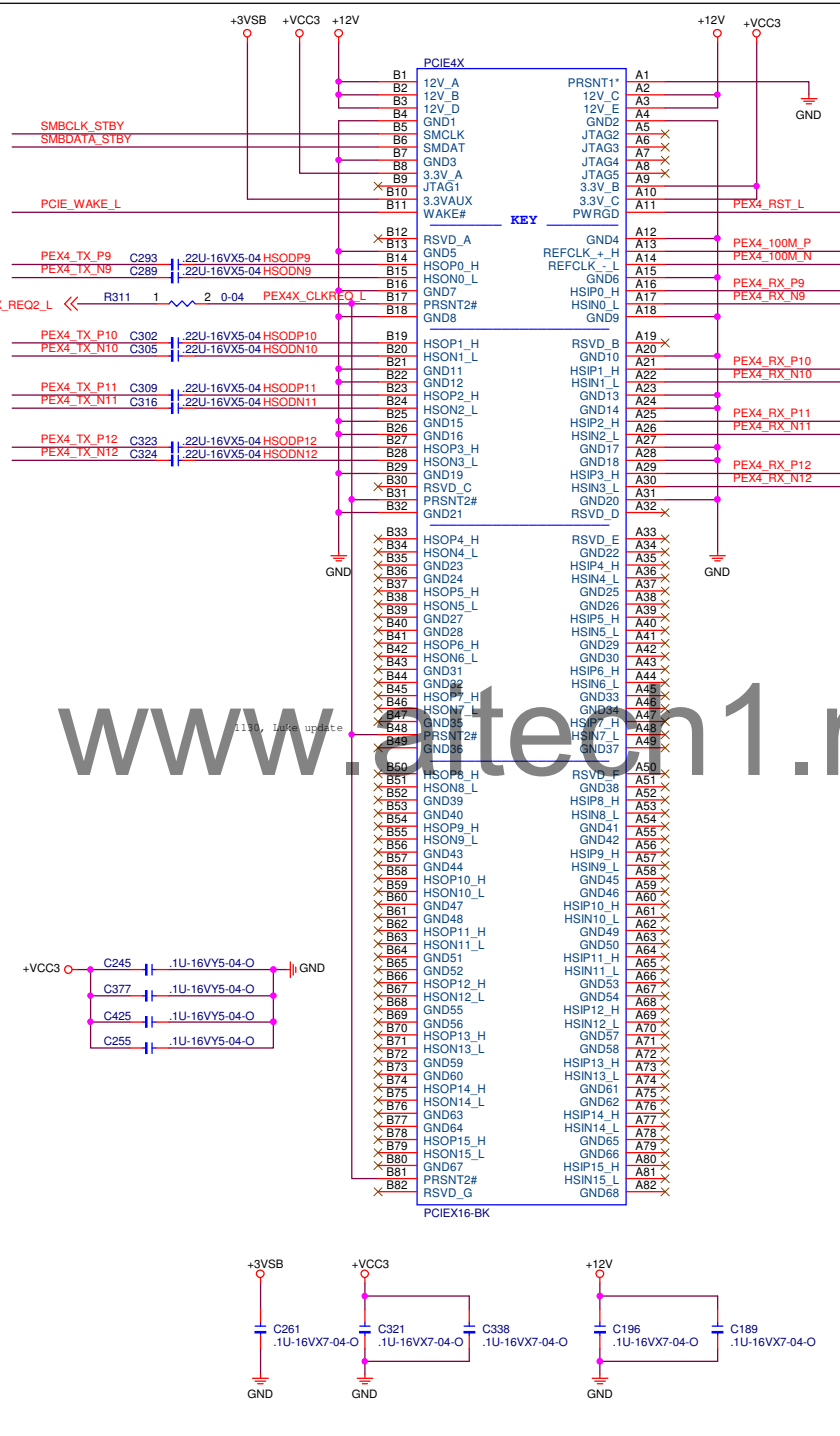
12,15,19,29,32,33 SMBCLK\_STBY  
12,15,19,29,32,33 SMBDATA\_STBY  
12,19,28 PCIE\_WAKE\_L

21 PEX4\_100M\_P  
21 PEX4\_100M\_N  
22 PEX4\_TX\_P9  
22 PEX4\_TX\_N9  
22 PEX4\_TX\_P10  
22 PEX4\_TX\_N10  
22 PEX4\_TX\_P11  
22 PEX4\_TX\_N11  
22 PEX4\_TX\_P12  
22 PEX4\_TX\_N12

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22 PEX4\_RX\_N9  
22 PEX4\_RX\_P10  
22 PEX4\_RX\_N10  
22 PEX4\_RX\_P11  
22 PEX4\_RX\_N11  
22 PEX4\_RX\_P12  
22 PEX4\_RX\_N12



21 PEX4X\_REQ2\_L



Between PCIeX4 & PCI



14 AD[31..0] << AD[31..0]  
 14 C\_BE\_L[3..0] << C\_BE\_L[3..0]

14 PME\_B\_L << PME\_B\_L  
 14 GNT0\_L << GNT0\_L  
 14 REQ0\_L << REQ0\_L

14 INTA\_L << INTA\_L  
 14 INTB\_L << INTB\_L  
 14 INTC\_L << INTC\_L  
 14 INTD\_L << INTD\_L

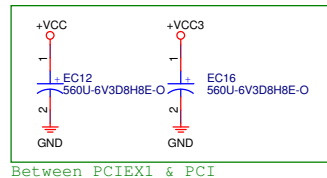
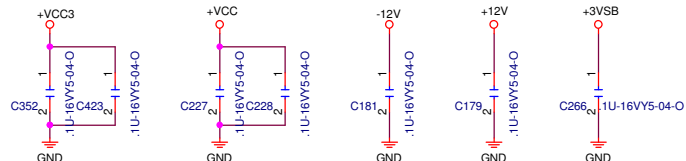
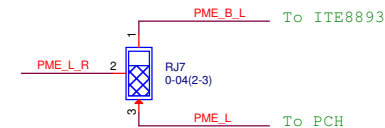
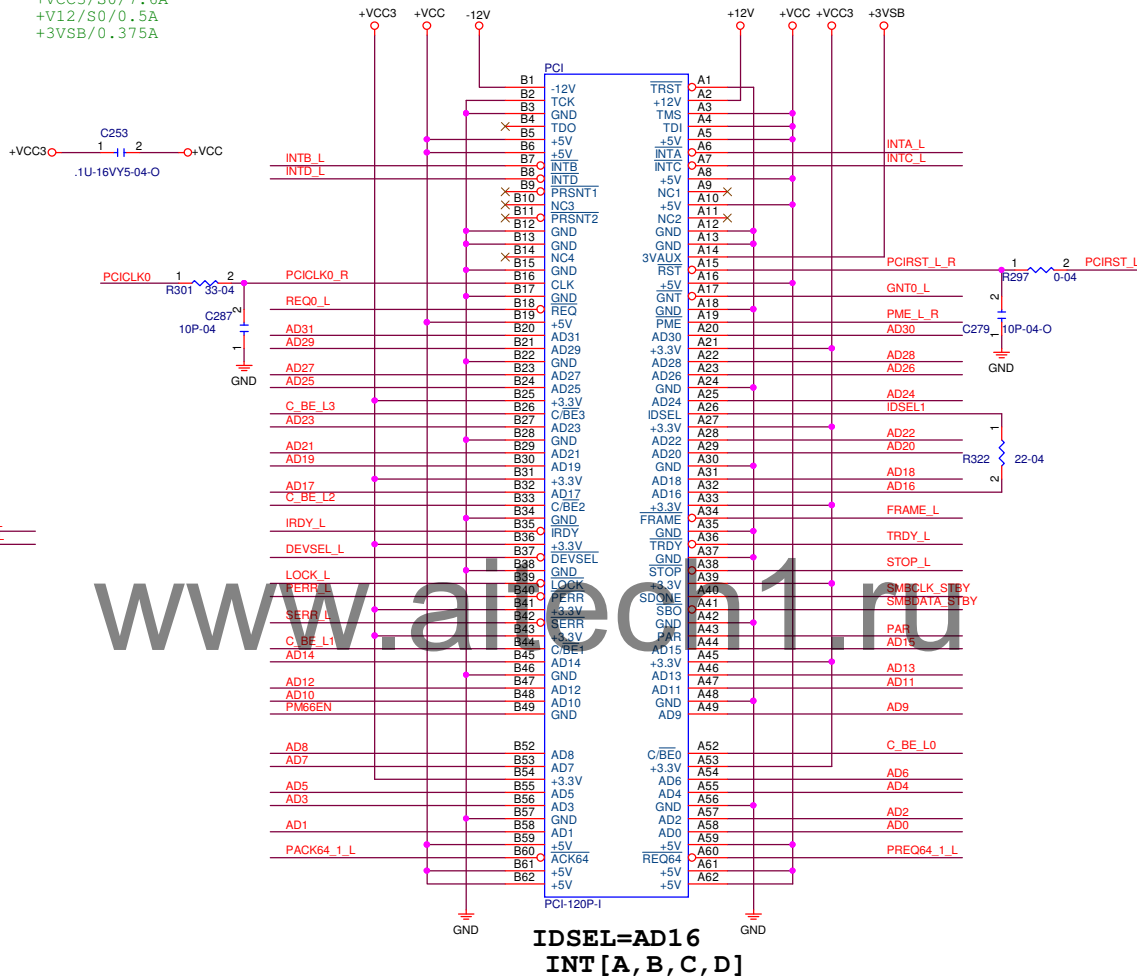
14 PAR << PAR  
 14 DEVSEL\_L << DEVSEL\_L  
 14 IRDY\_L << IRDY\_L  
 20 PME\_L << PME\_L  
 14 SERR\_L << SERR\_L  
 14 STOP\_L << STOP\_L  
 14 LOCK\_L << LOCK\_L  
 14 TRDY\_L << TRDY\_L  
 14 PERR\_L << PERR\_L  
 14 FRAME\_L << FRAME\_L

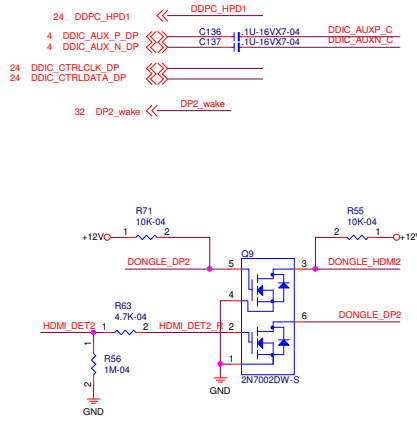
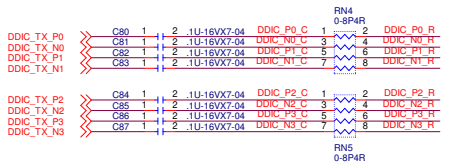
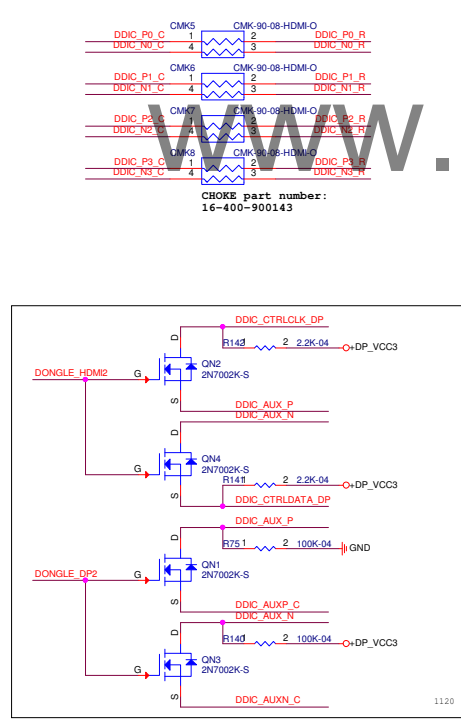
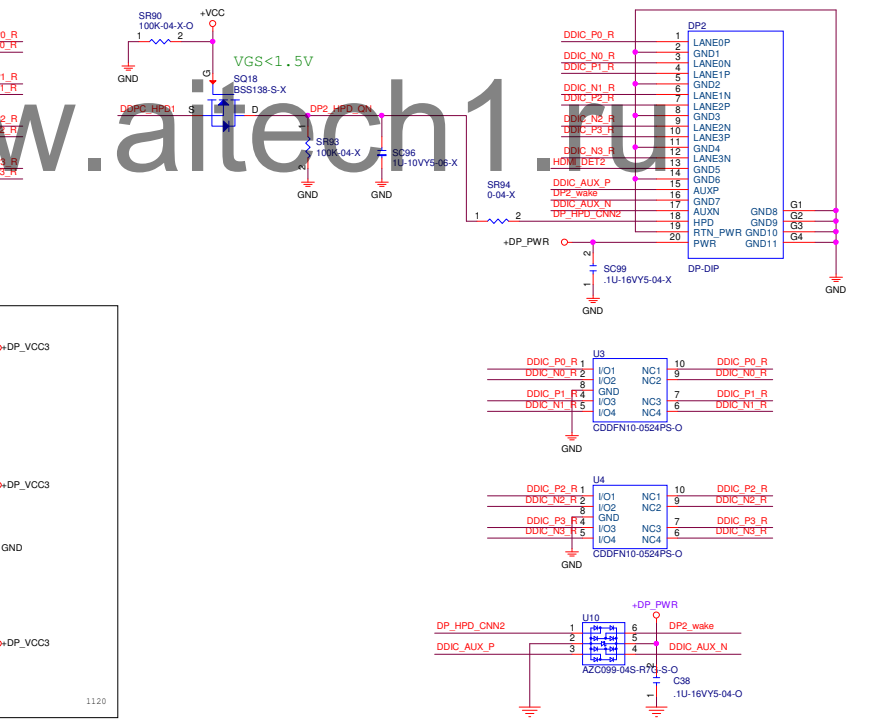
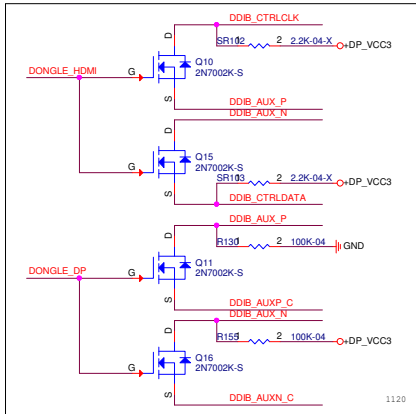
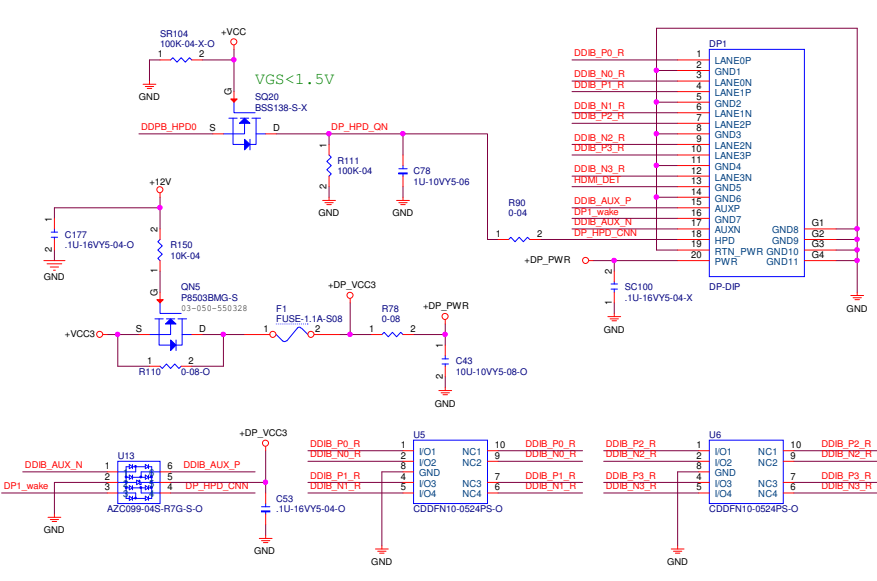
14 PCIRST\_L << PCIRST\_L  
 14 PCICLK0 << PCICLK0  
 14 PM66EN << PM66EN

12,13,19,29,32,33 SMBCLK\_STBY << SMBCLK\_STBY  
 12,13,19,29,32,33 SMBDATA\_STBY << SMBDATA\_STBY

\*\*PCI Slot\*\*  
 +VCC/S0/5A  
 +VCC3/S0/7.6A  
 +V12/S0/0.5A  
 +3VSB/0.375A

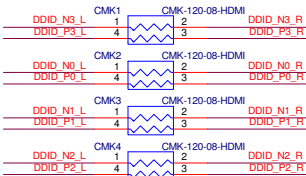
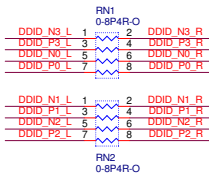
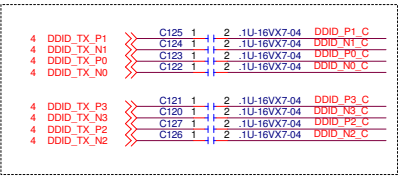
+VCC3 R412 1 2 8.2K-04 PACK64\_1\_L  
 R411 1 2 8.2K-04 PREQ64\_1\_L



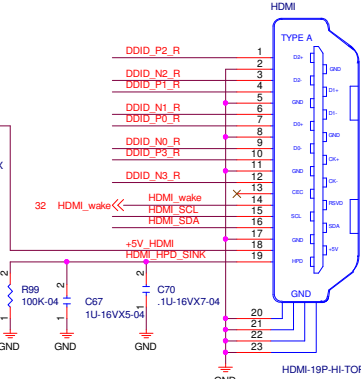
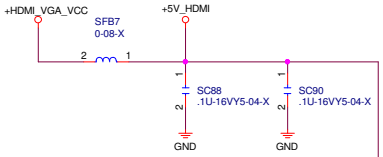




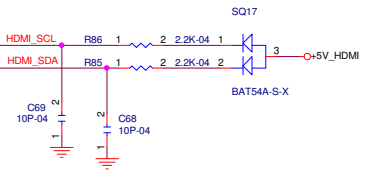
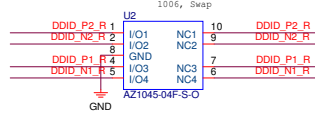
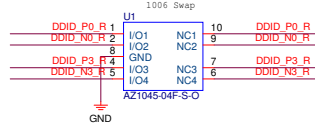
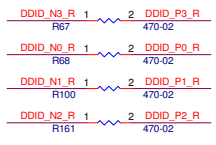
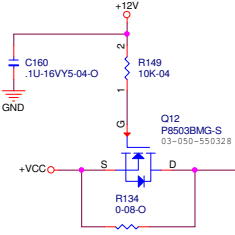
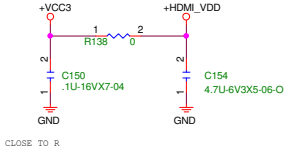
HDMI



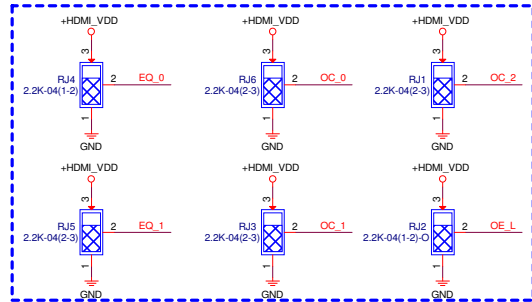
CHOKE part number:  
16-400-121143



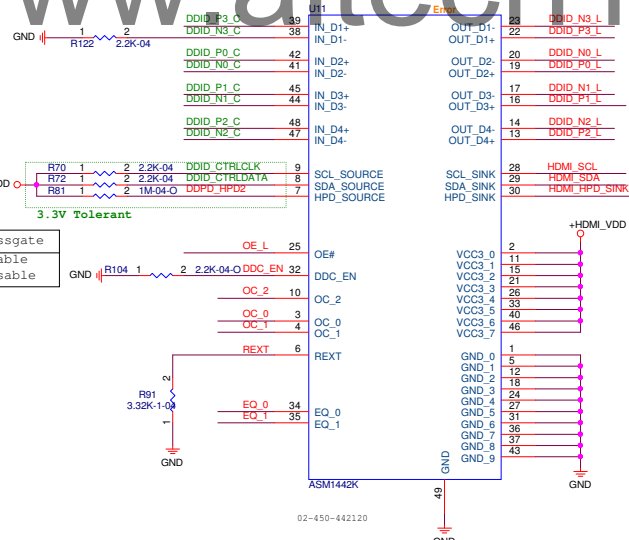
HDMI Connector Pin13:CEC  
沒有使用必須空接(Floating)  
避免HDCP測試 FAIL



www.aitech1.ru



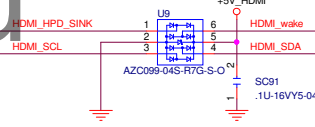
RQ1=1, RQ0=0 for 4K2K. 201702232, CG0=1,CG1=1,CG2=1 for SI

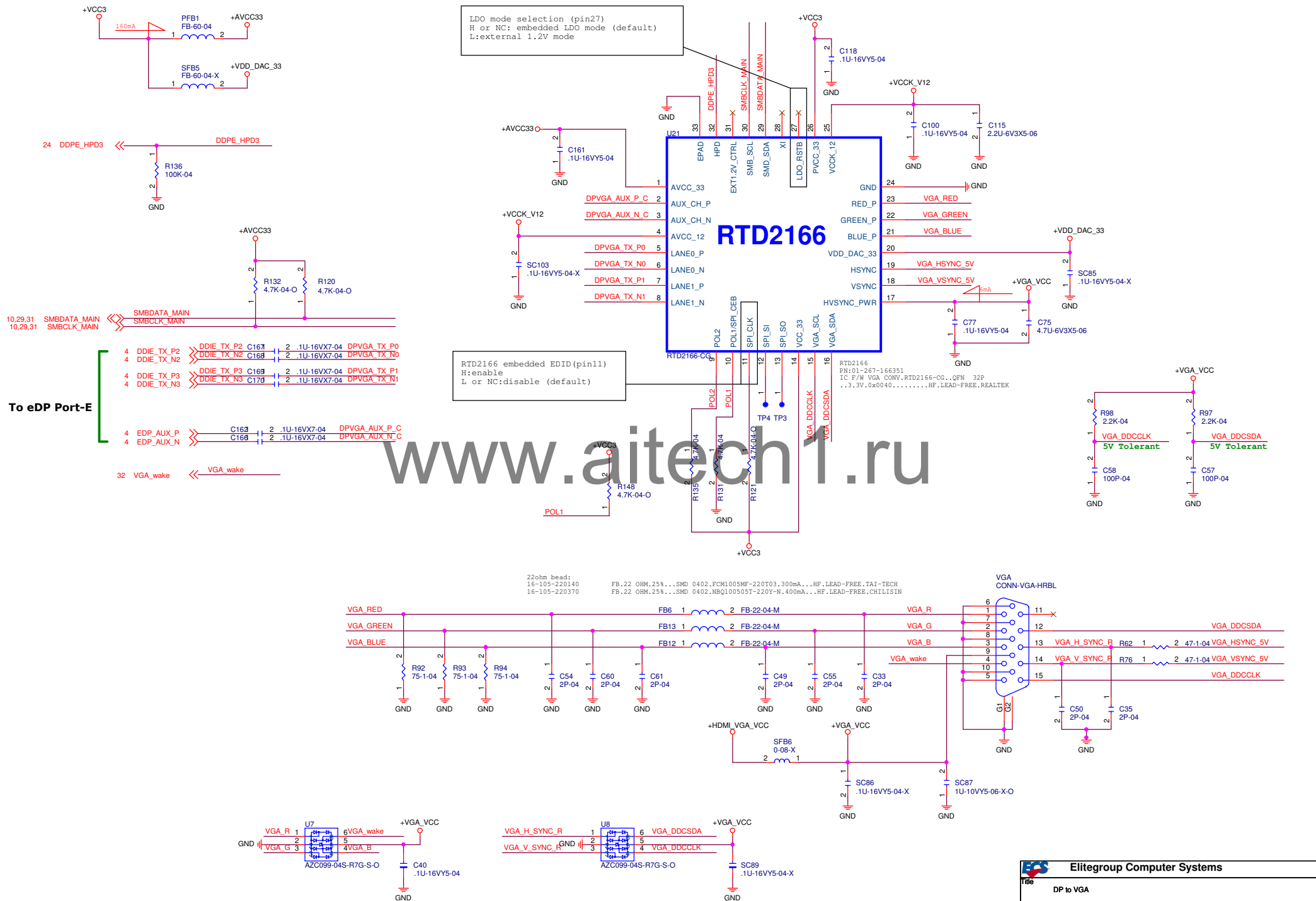


5V Tolerant

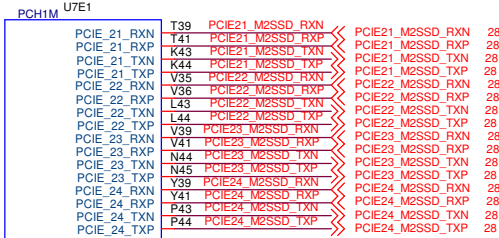
HD_HPD	Status
Hi	Plugged
Lo	unplugged

HD\_HPD:Internal 100K pull low

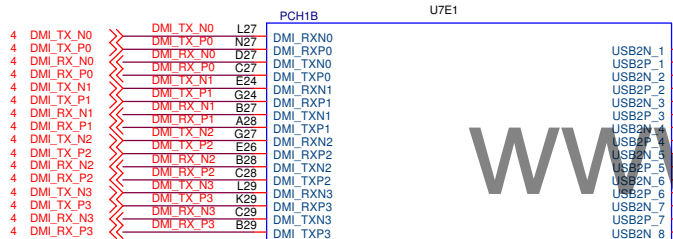
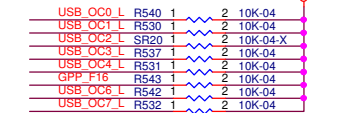
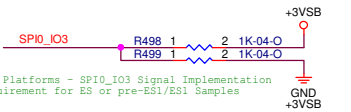
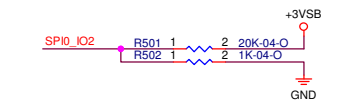
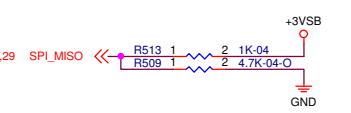
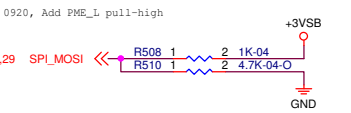
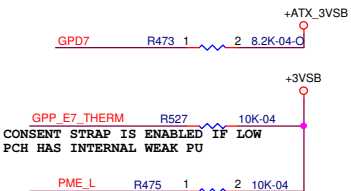
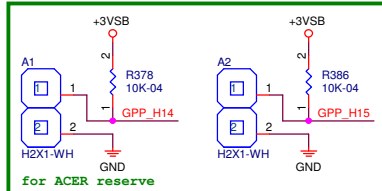
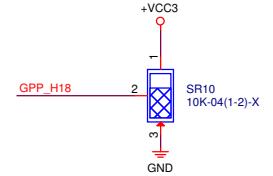
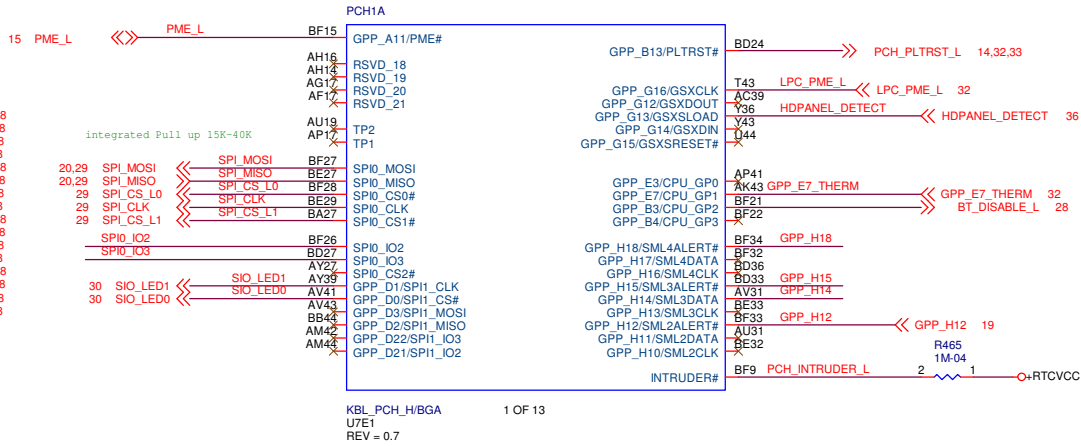








19 OF 19  
KBL\_PCH\_H/BGA  
REV = 0.7



Front IO USB3.0 for Q270 only

INT D Intel LAN

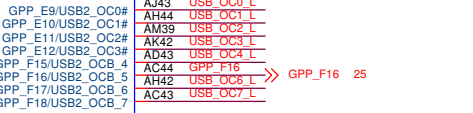
PCI

INT B Realtek LAN

M.2

PCIe X1

- Front CR
- Rear IO USB2\_LAN
- Rear IO USB3.0x4
- WLAN
- Front USB2.0
- Front USB3.0 (1.5A)
- Front USB2.0
- Front USB3.0 (1.5A)
- Rear IO USB3.0x4
- Front USB3.0

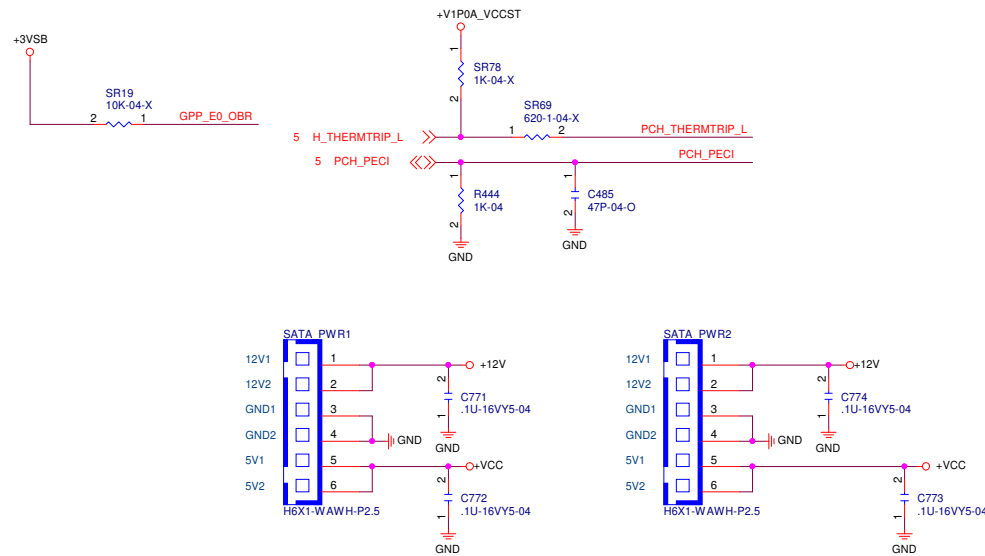
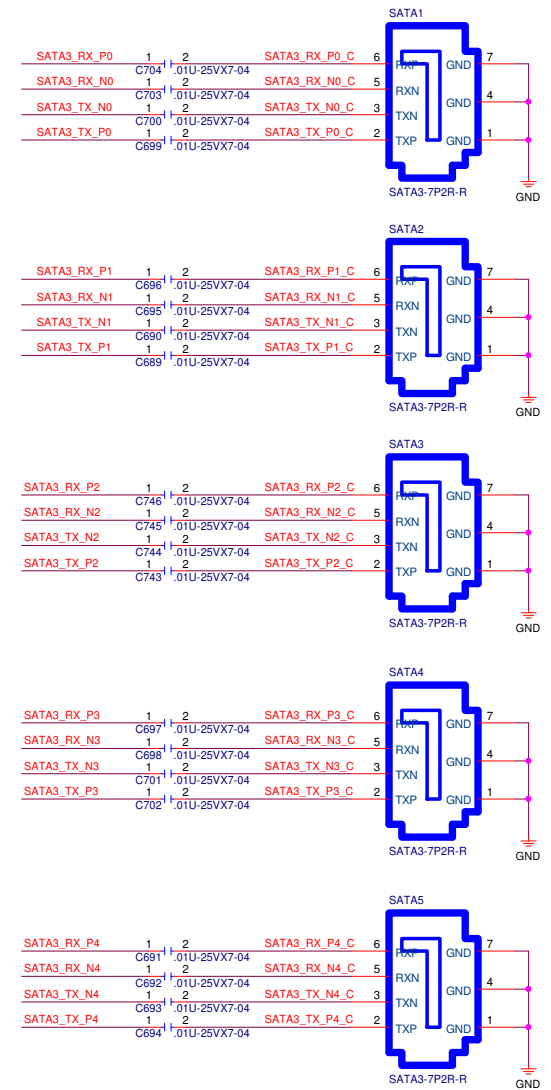


KBL\_PCH\_H/BGA

REV = 0.7

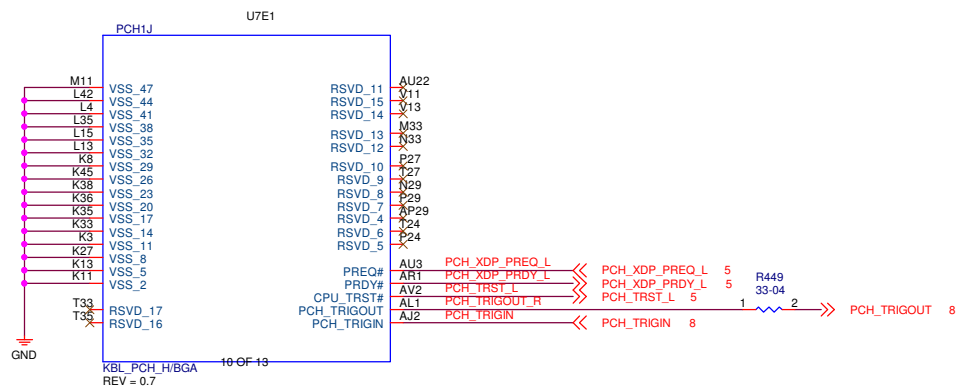
2 OF 13



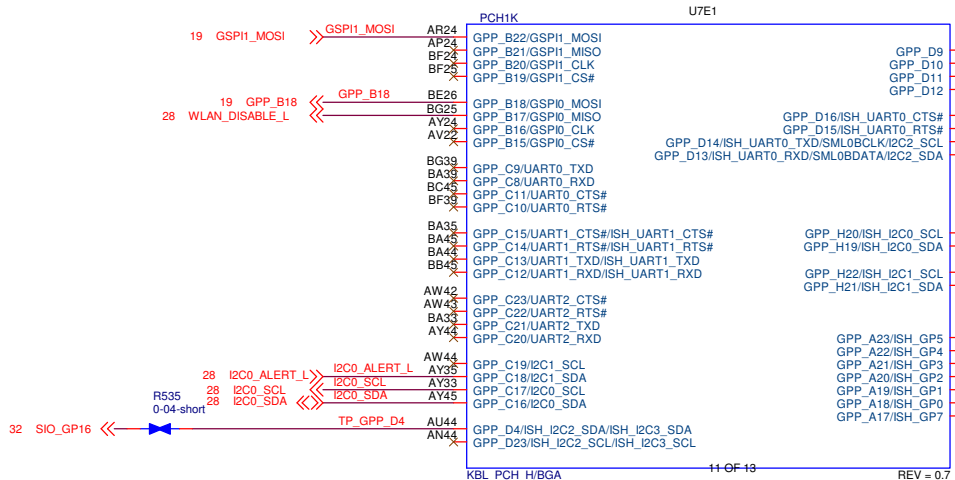
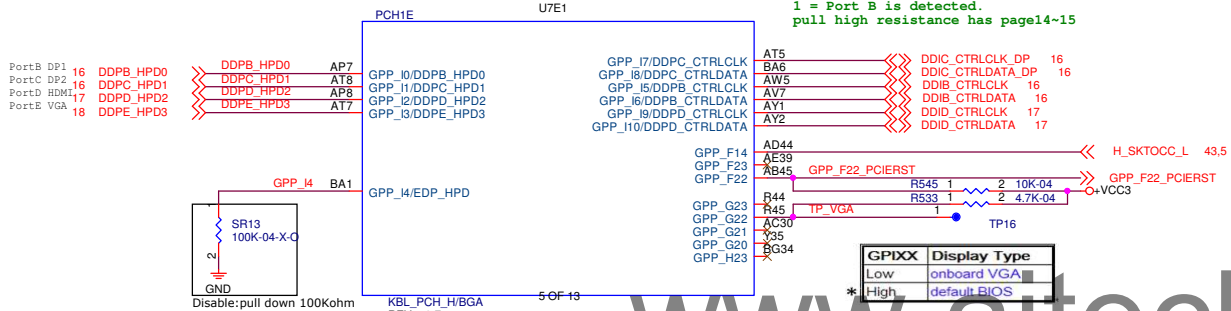


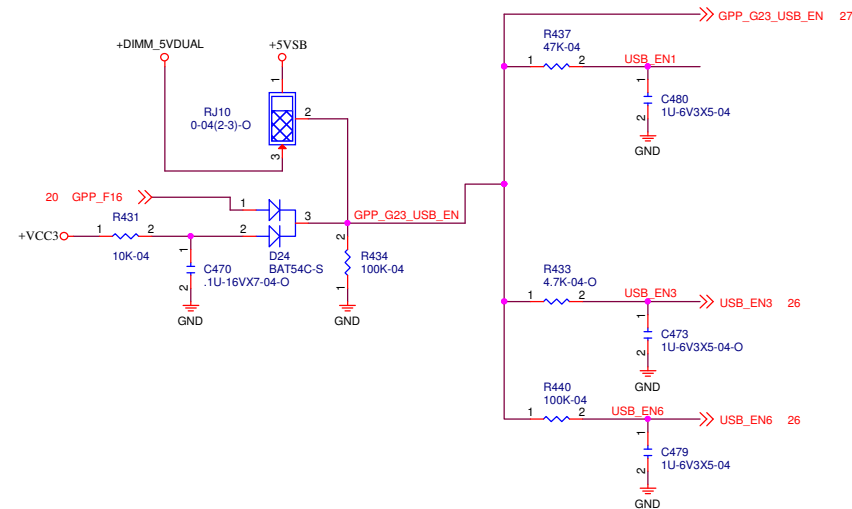






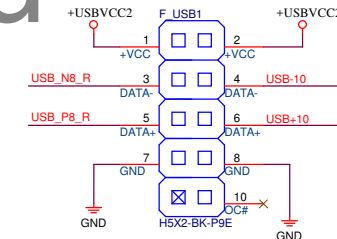
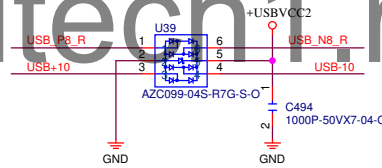
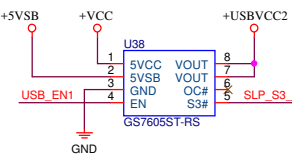
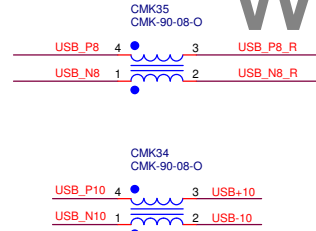
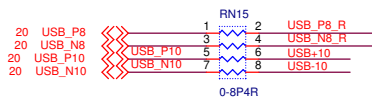
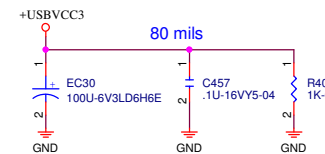
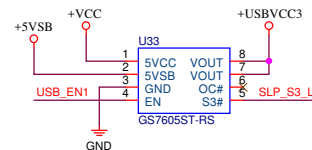
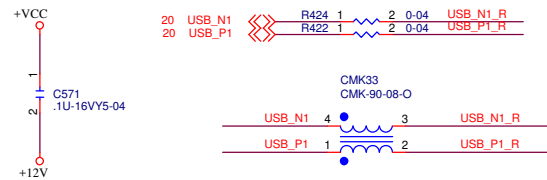
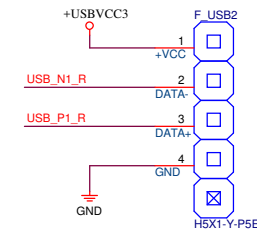
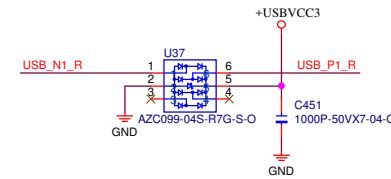
Display Port B/C/D Detected  
This signal has a weak internal pull-down.  
0 = Port B is not detected.  
1 = Port B is detected.  
pull high resistance has page14~15



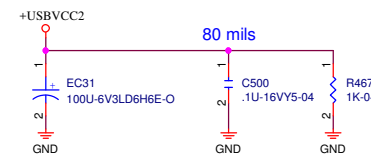
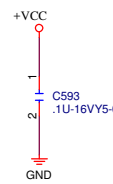
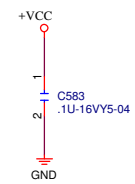
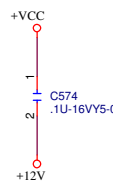


	power switch Enable use	RJ5	D26	S4/S5 USB_5V_DUAL	Customer
	VDIMM	0ohm (2-3)	NA	0 Volt	Acer S4 W S5 W/O USB_5VDUAL
	5VSB	0ohm (1-2)	NA	5 Volt	
*	GPIO	NA	Stuff	S4 : 5 Volt S5 : 0 Volt	

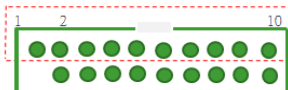
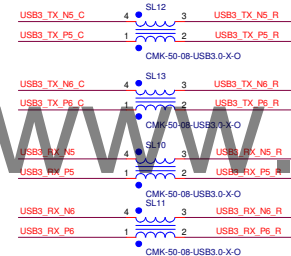
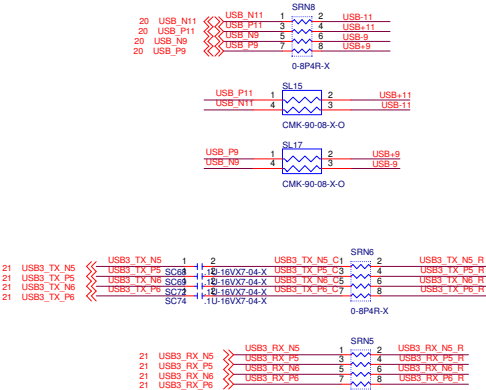
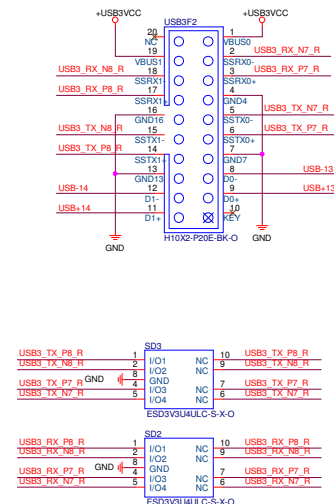
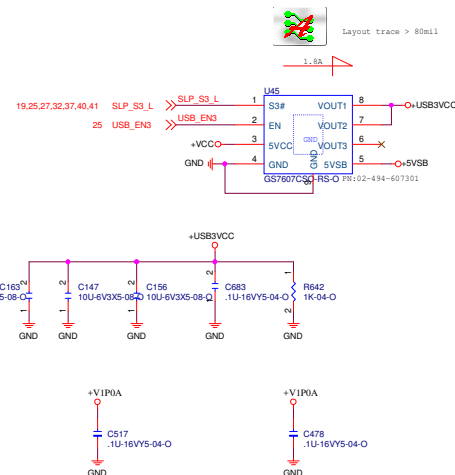
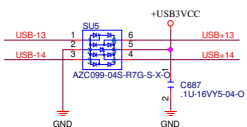
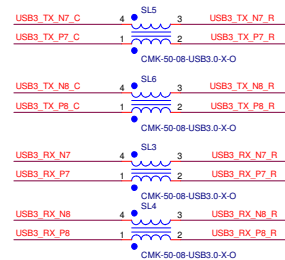
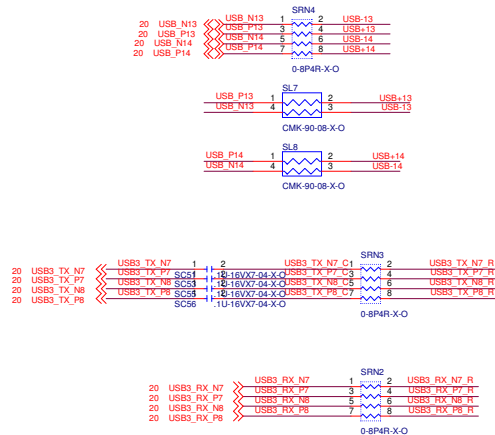
STATUS	S0	S3	S4	S5
GPP_F16	HI	HI	HI	LOW
USB_PWR	ON	ON	ON	OFF



19,26,27,32,37,40,41 SLP\_S3\_L SLP\_S3\_L

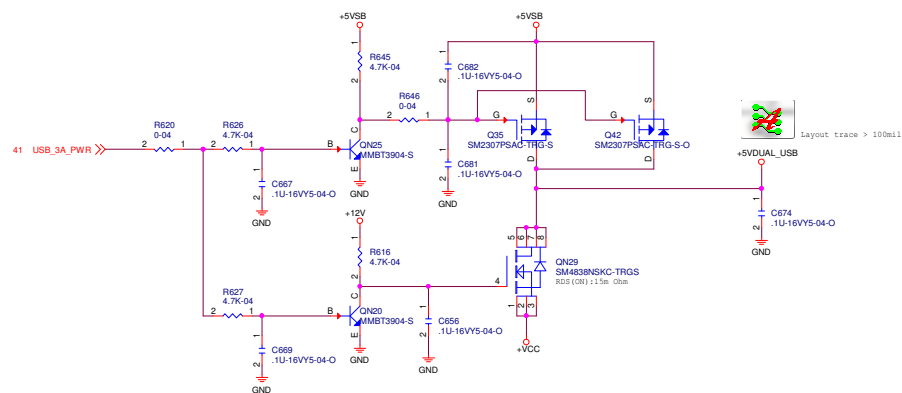
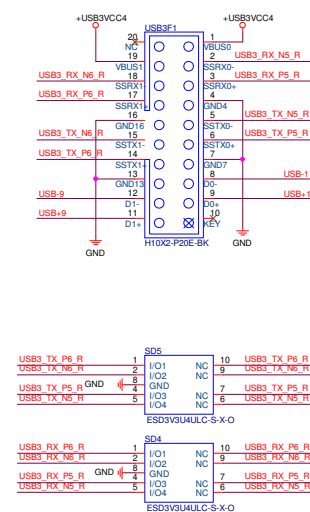
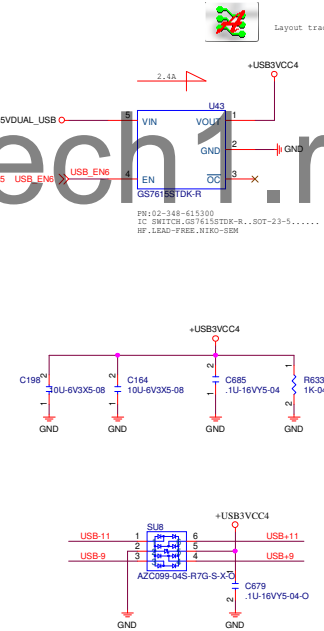



For Q270 only

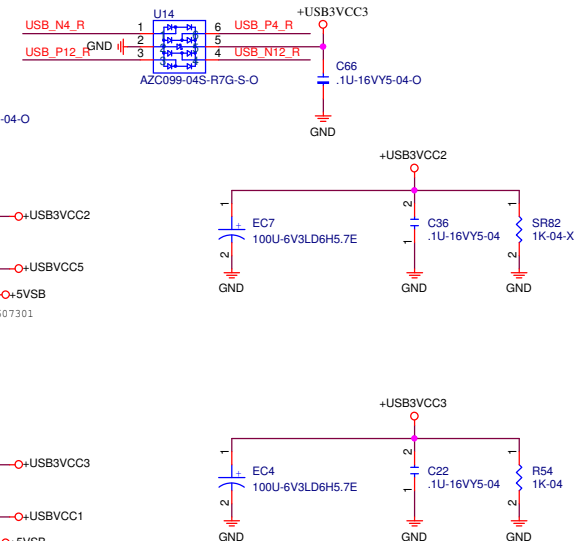
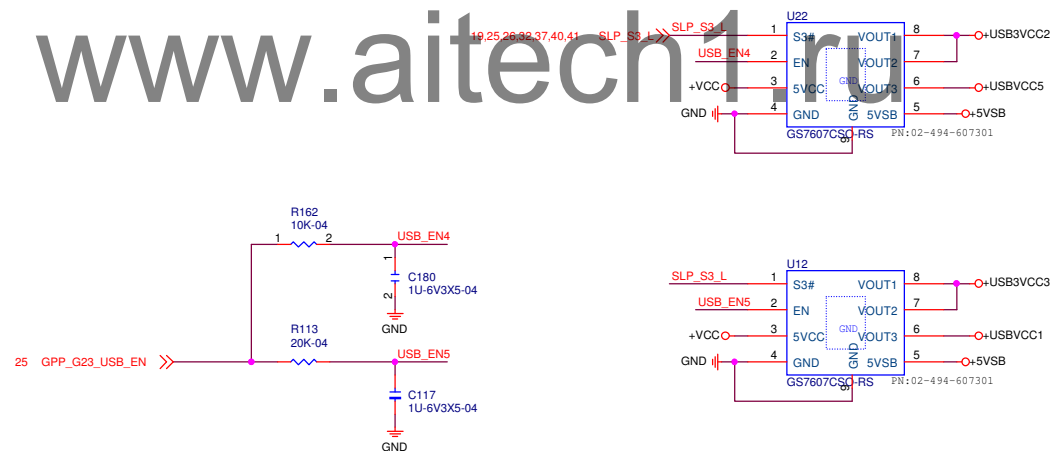
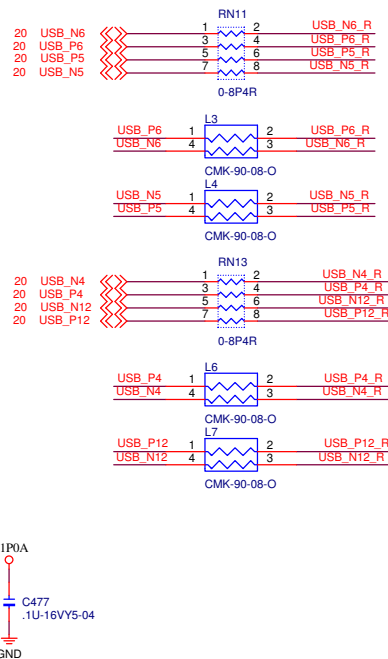
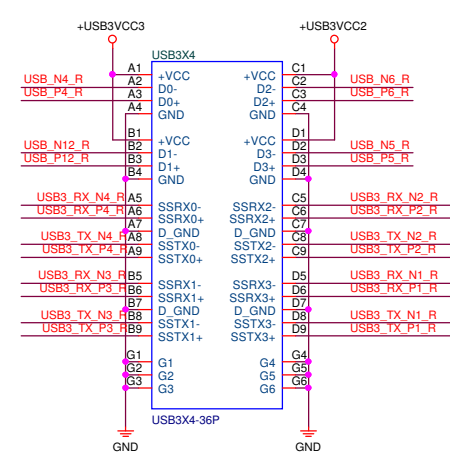
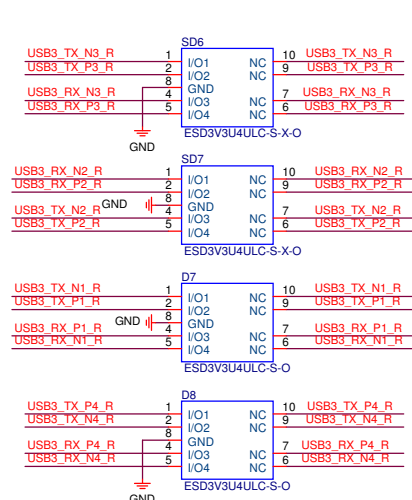
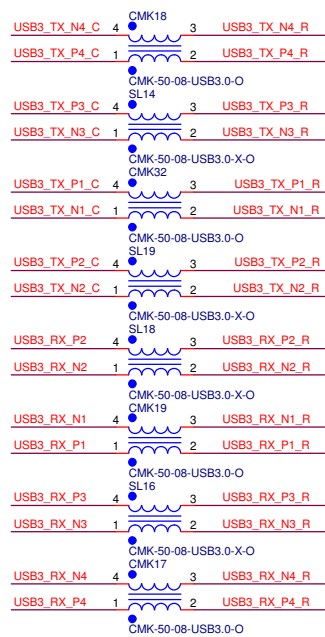
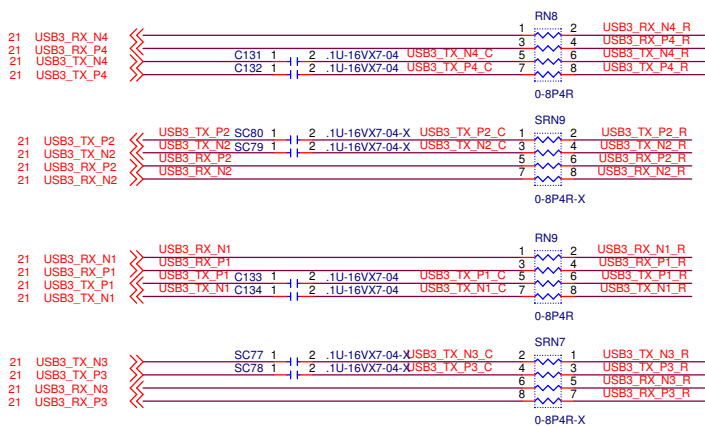


- USB Port0  
(USB Type-C)

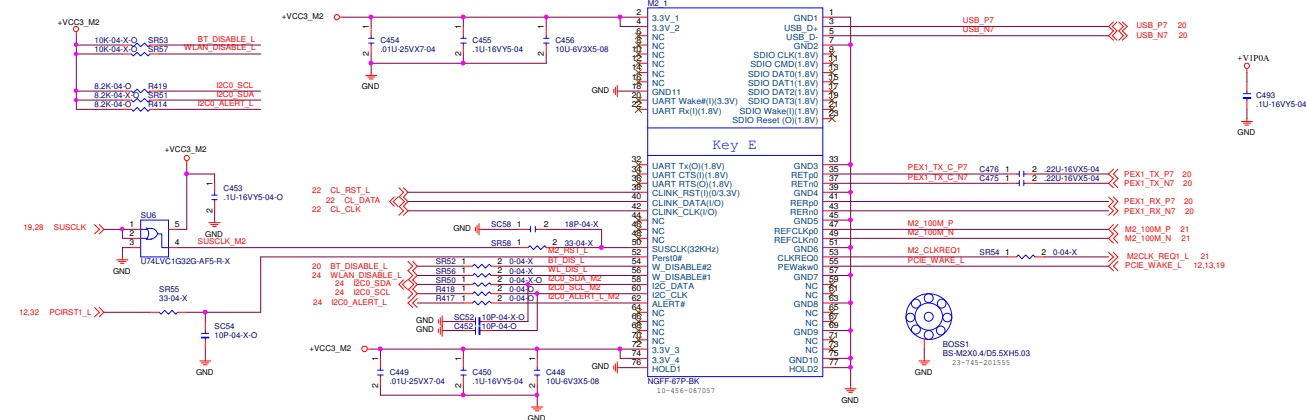
USB Port 1



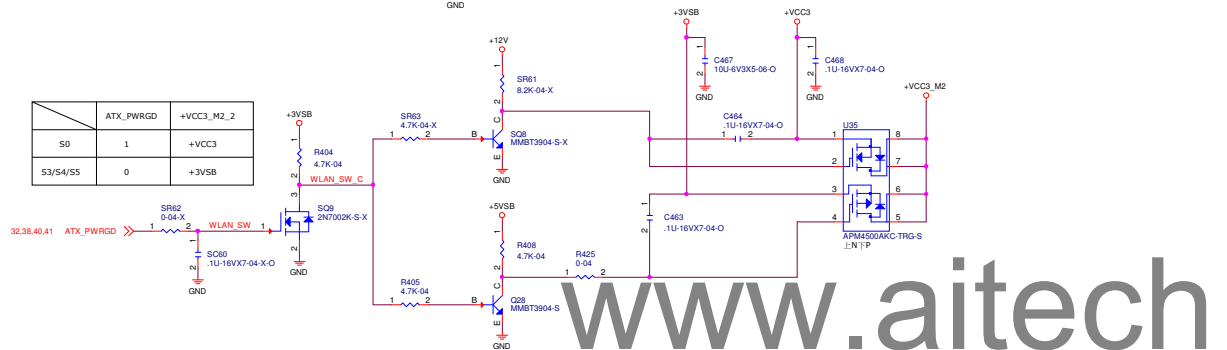
 <b>Elitegroup Computer Systems</b>			
Title			
USB3.0 Header*2			
Size	Document Number		Rev
Custom	B25H4-AM		1
Date:	Thursday, March 30, 2017	Sheet	26 of 49



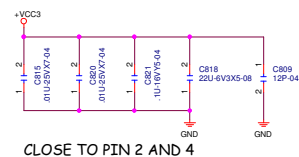
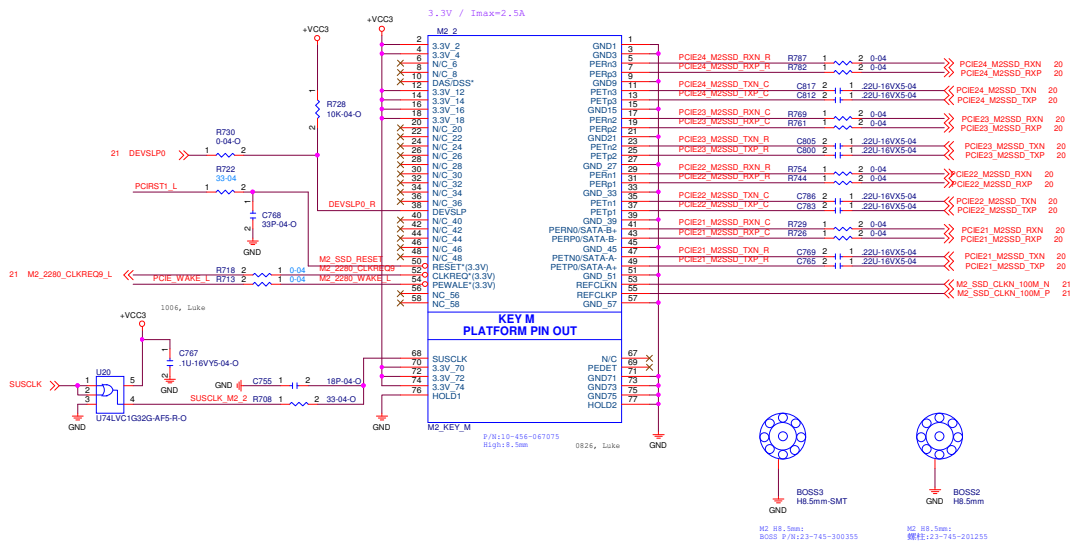
## M.2 WIFI



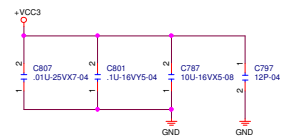
	ATX_PWRGD	+VCC3_M2_2
S0	1	+VCC3
S3/S4/S5	0	+3VSB



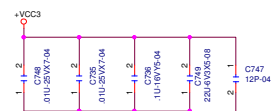
## M.2 SSD



CLOSE TO PIN 2 AND 4



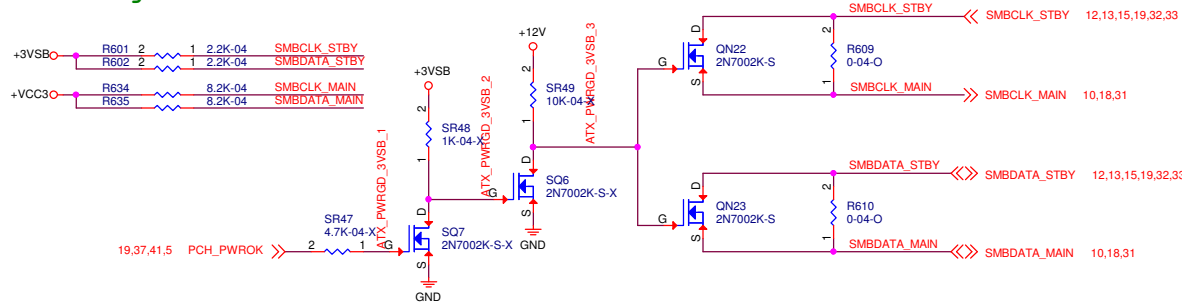
CLOSE TO PIN 12,14,16 AND 18



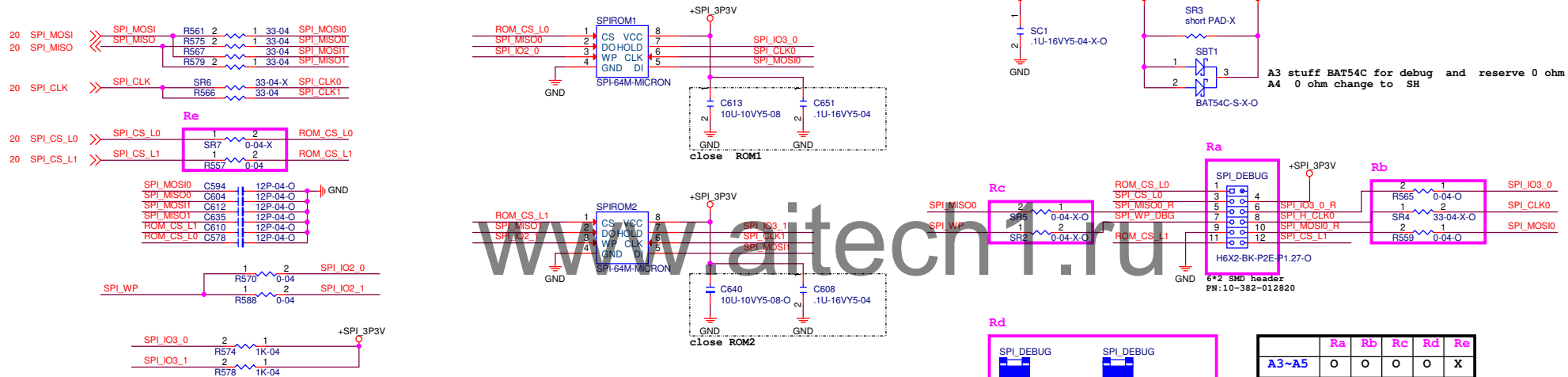
CLOSE TO PIN 70 72 AND 74



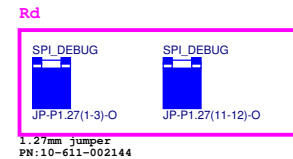
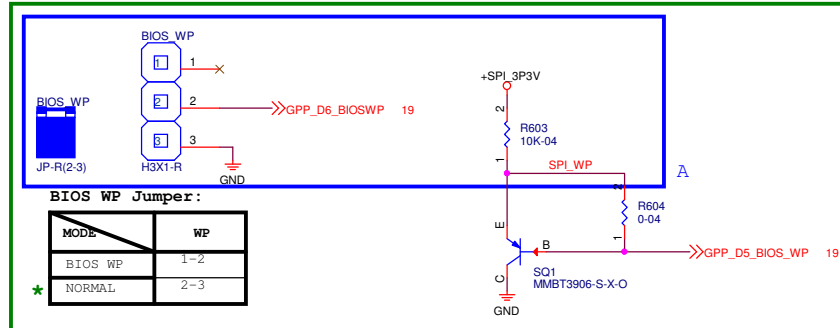
## SMBus Logic Circuit



## SPI ROM



## BIOS WP

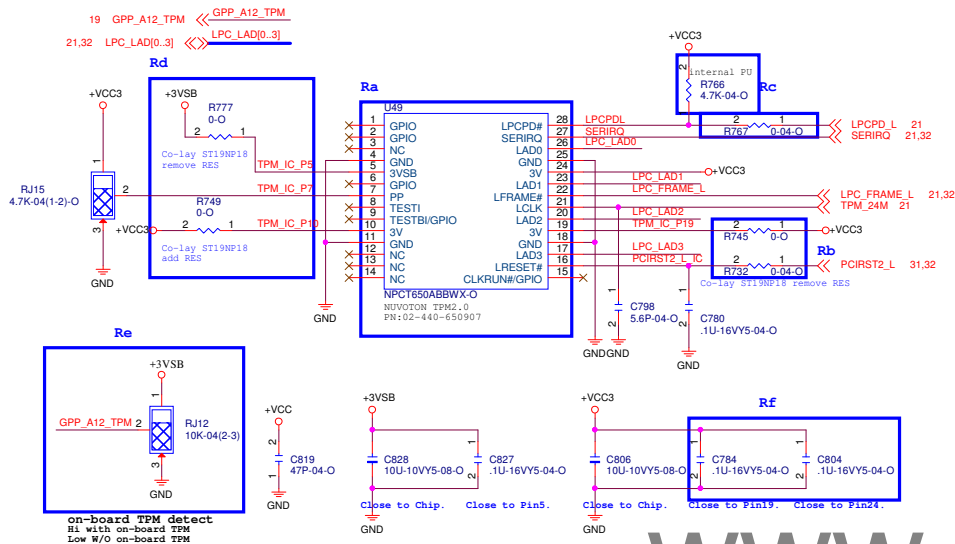


	Ra	Rb	Rc	Rd	Re
A3~A5	O	O	O	O	X
MP	X	X	X	X	O

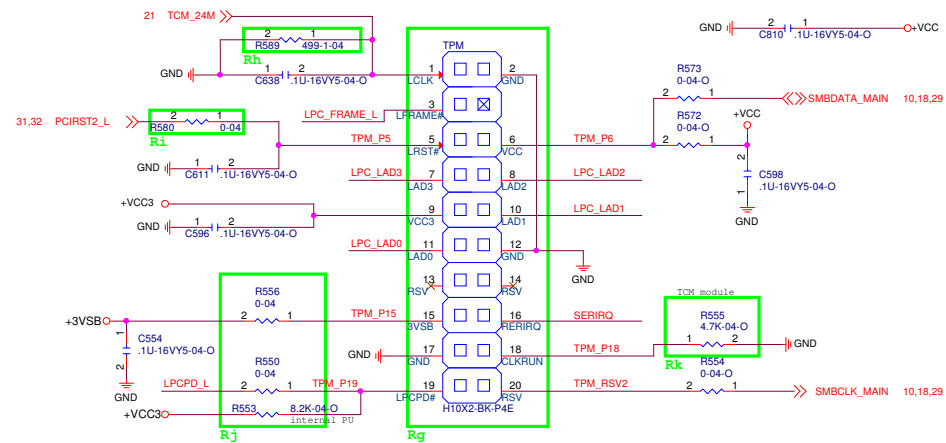


## TPM chip/header circuit

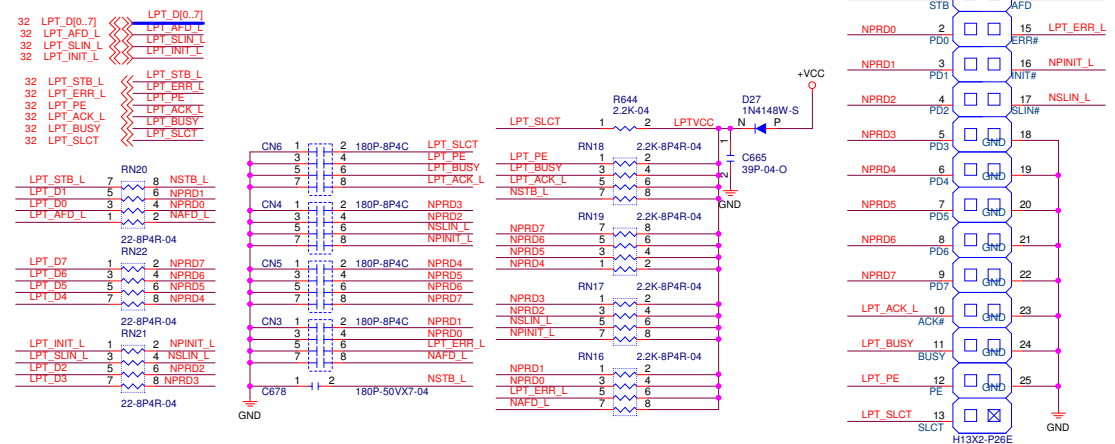
	Ra-Rf IC						Rg-Rk Header				
<b>Q270</b>	Ra	Rb	Rc	Rd	Re	Rf	Rg	Rh	Ri	Rj	Rk
for Acer	O	O	O	O	(1-2)	O	X	X	X	X	X
<b>B250</b>	Ra	Rb	Rc	Rd	Re	Rf	Rg	Rh	Ri	Rj	Rk
for Acer Founder	X	X	X	X	(2-3)	X	O	O	O	O	O



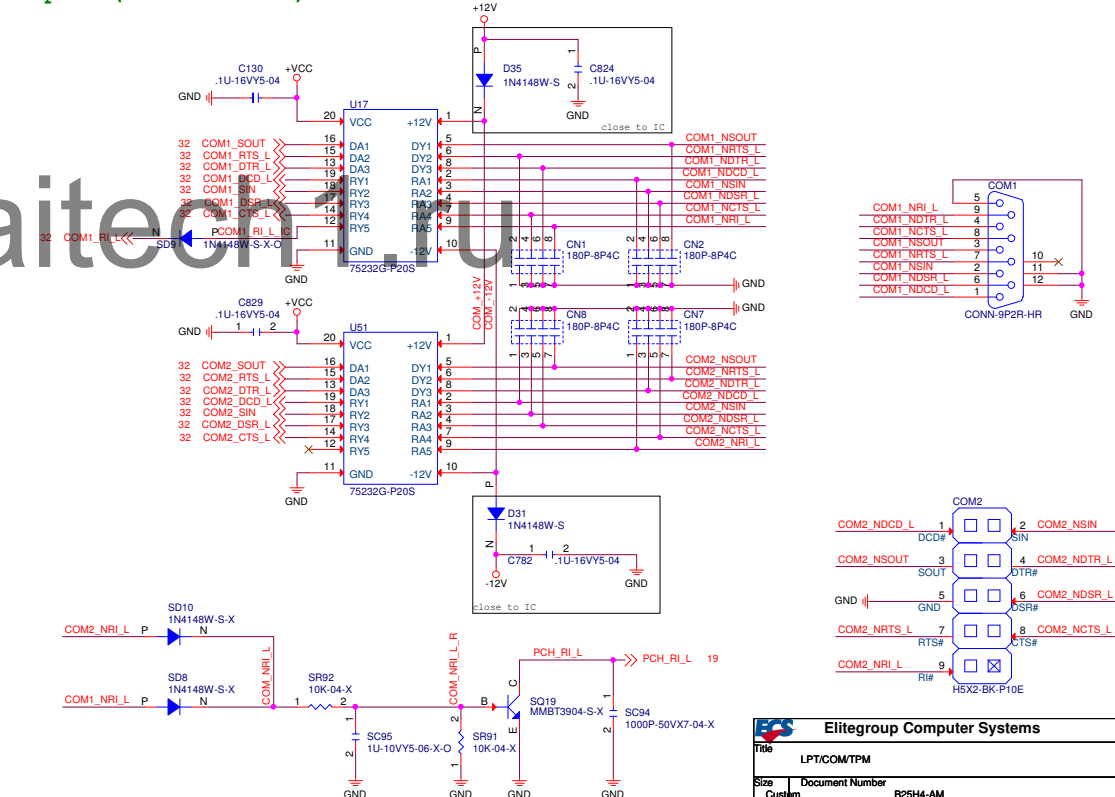
For B250

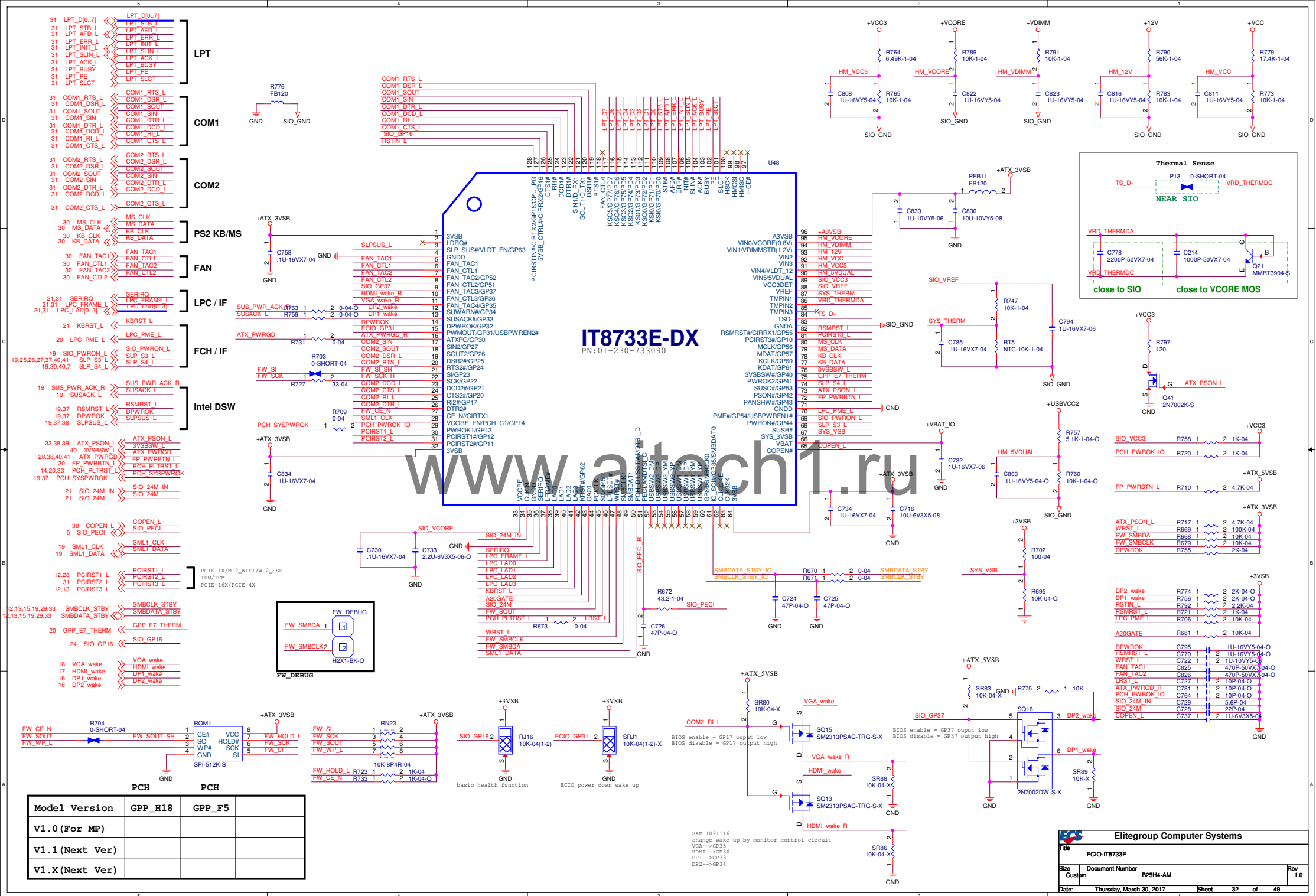


## LPT Header

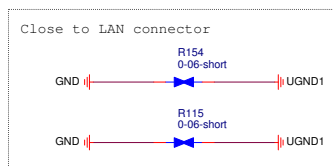
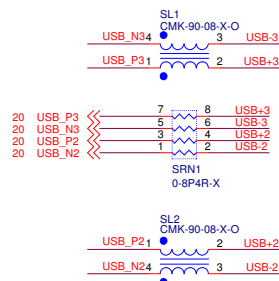
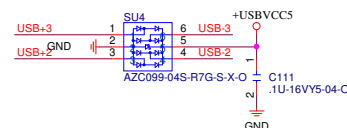
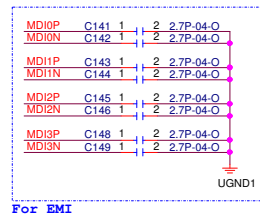


COM port (conn & header)



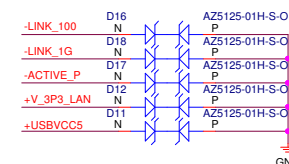
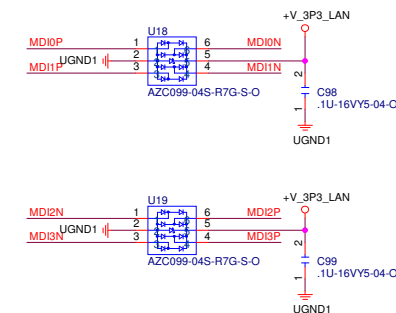
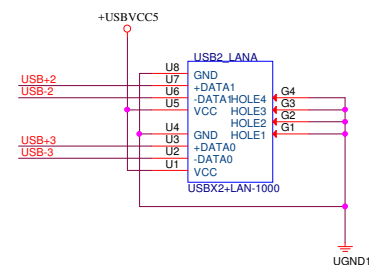






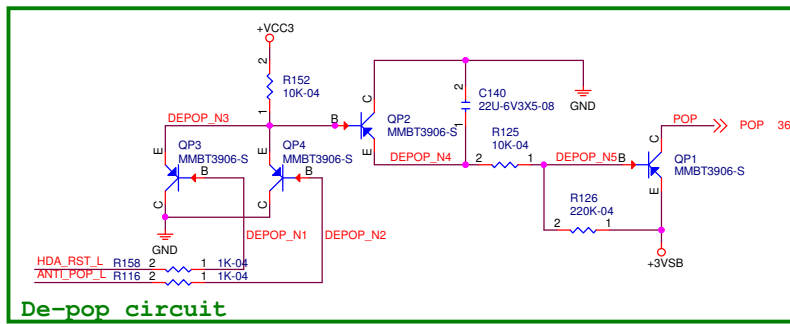
The schematic diagram illustrates the electrical connections for the USB2+LAN module. Key components and connections include:

- USB2+LAN Module:** Features pins P1 through P9, GLED, GLED+, GLED-, G5, G6, G7, G8, and DGND. It contains a USB2+LAN-1000 chip and a LAN9304 chip.
- RJ45 P19:** Connected to MDIOP, MDION, MDIP, MDI1N, MDI2P, MDI2N, MDI3P, and MDI3N.
- LEDs:** LED2 is connected to R123 (150Ω), LED1 to R137 (150Ω), and LED0 to R147 (330Ω).
- Power and Grounding:** C103 (1U-16VY5-04) is connected to UGND1. C108, C102, and C129 (740P-50VX7-04) are connected to GND and UGND1.
- Other Connections:** -LINK\_100, -LINK\_TG, and -ACTIVE\_P are connected to G5, G6, and G7 respectively. DGND is connected to P10 and R101 (100Ω).

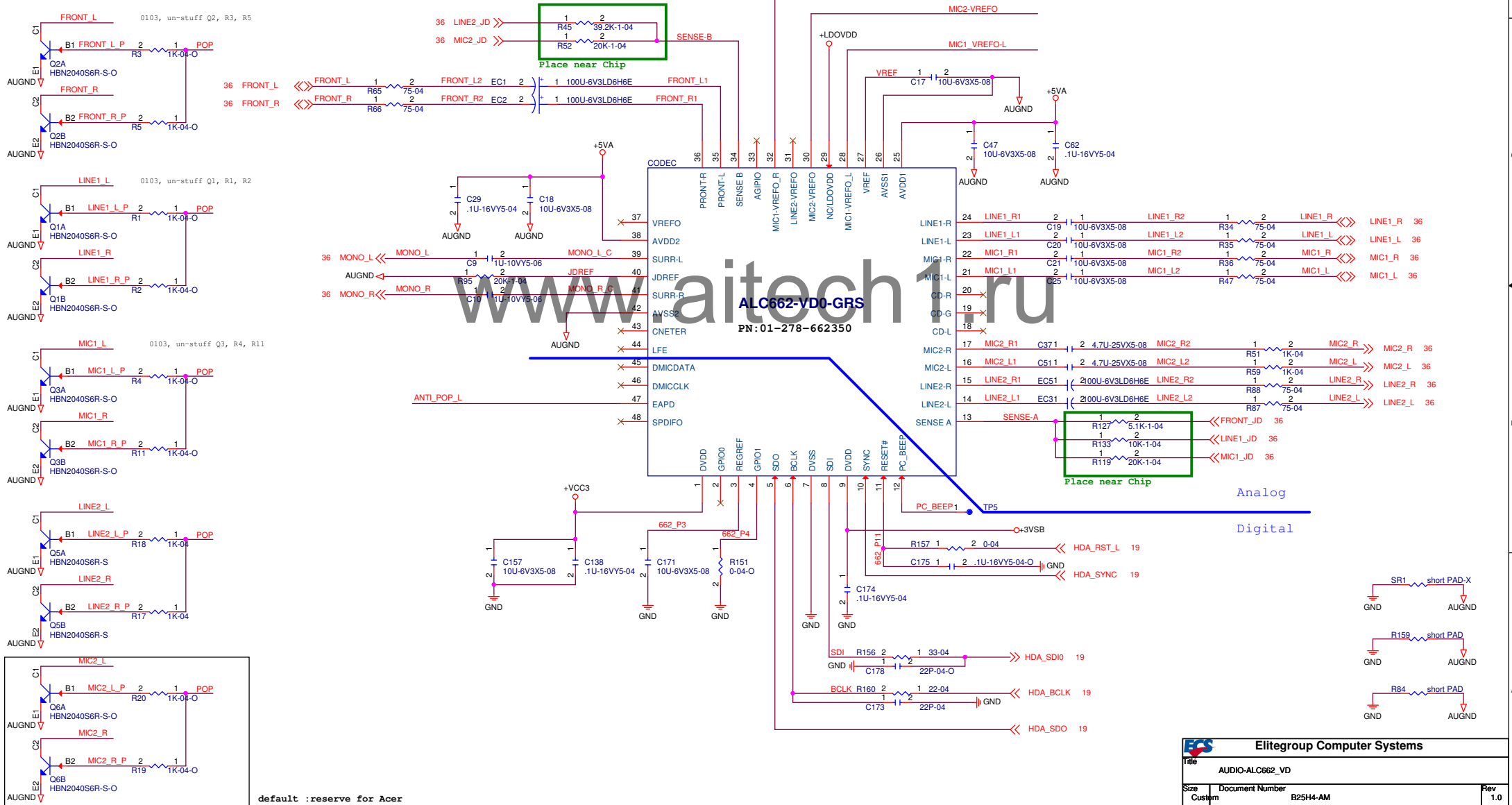
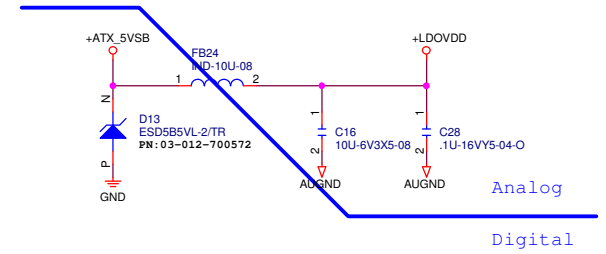
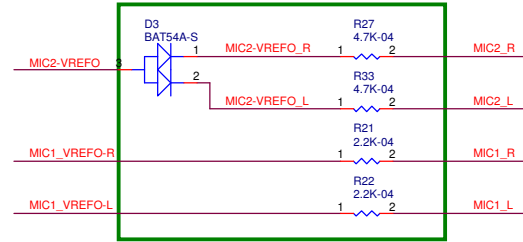


				S0	S3	S4	S5	G3 to 8
<div>Rear Side</div> <div>ActiveSpeed</div>	Active LED (Single Color)	Access	Blink	Blink	Blink	Blink		
		Not Access	OFF	OFF	OFF	OFF		
	Speed-LED (Dual Color)	Disconnected	OFF					
		1000: ON with Amber Color	ON	OFF	OFF	OFF		
		100: ON with Green Color	ON					
		10: OFF	OFF					

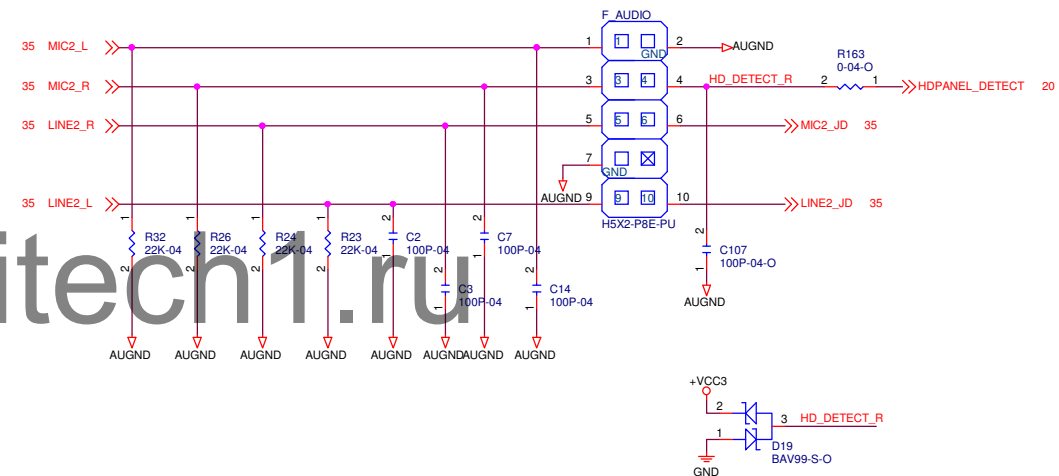
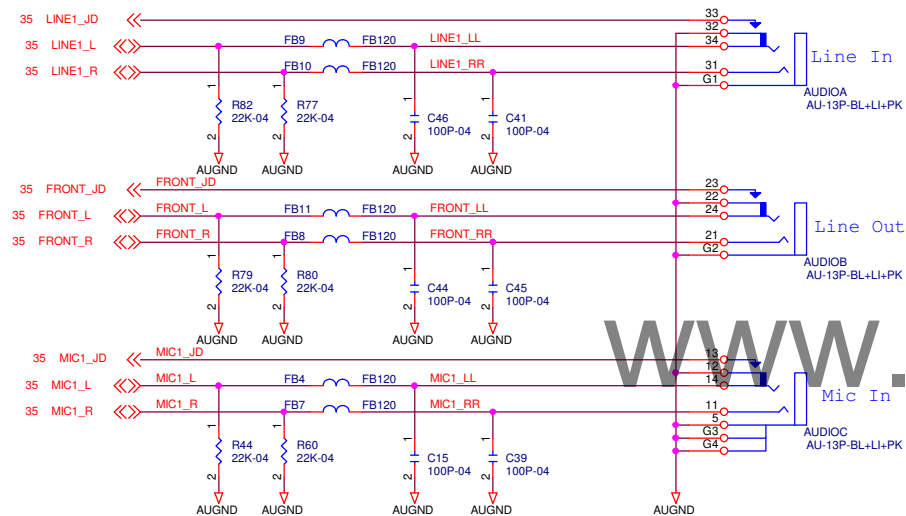
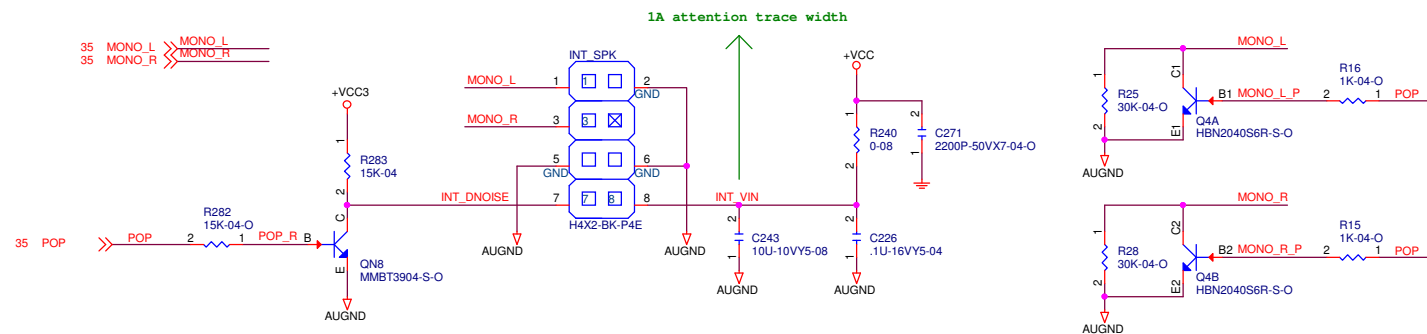




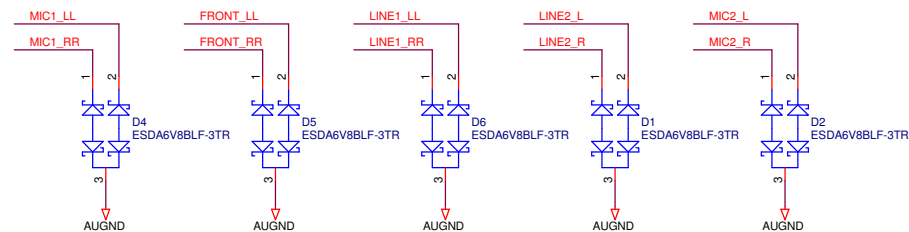
## MIC Bias



Elitegroup Computer Systems			
Title			
AUDIO-ALC662_VD			
Size			
Custom	Document Number	B25H4-AM	Rev 1.0
Date:			
Monday, March 06, 2017			
Sheet			
35 of 49			

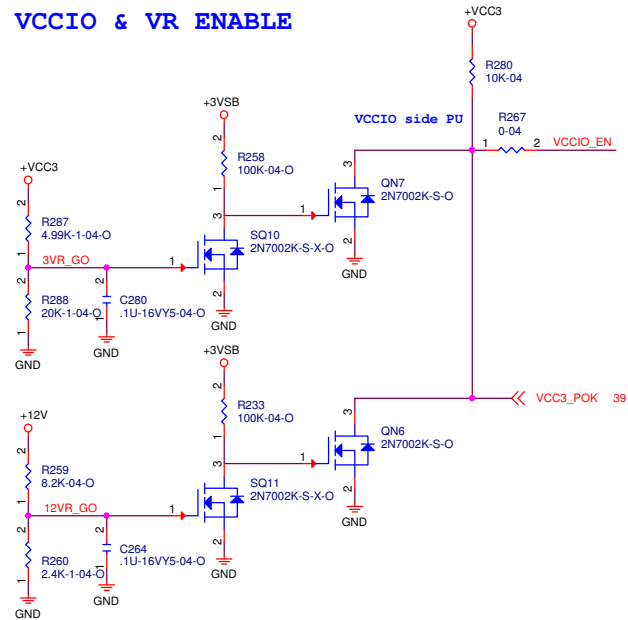


A	B	C
	PIN	FUNCTION
LINE IN	3Q	LINE IN-JD
	3P	AUGND
	31	LINE IN_L
	34	LINE IN_R
	G1	AUGND
LINE OUT	2Q	LINE OUT-JD
	2P	AUGND
	21	LINE OUT_L
	24	LINE OUT_R
	G2	AUGND
MIC IN	1Q	MIC IN-JD
	1P	AUGND
	11	MIC IN_L
	14	MIC IN_R
	5	AUGND

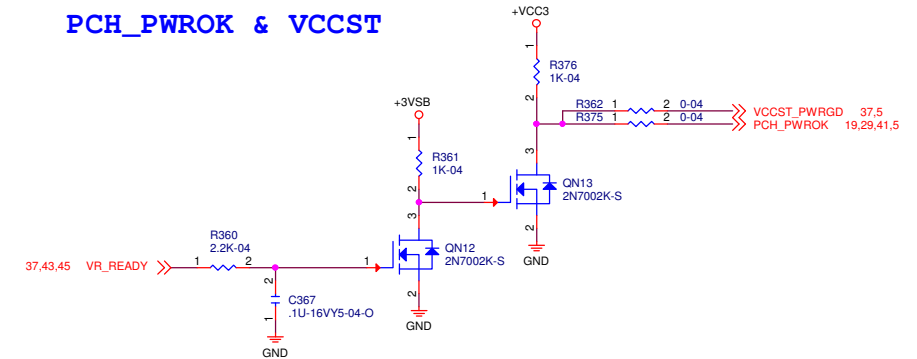


PN:03-100-700872  
TVS ARRAY..ESDA6V8BLF-3/TR..SOT-23.5V.....LEAD-FREE (RoHS/HF) .WILLSEMI

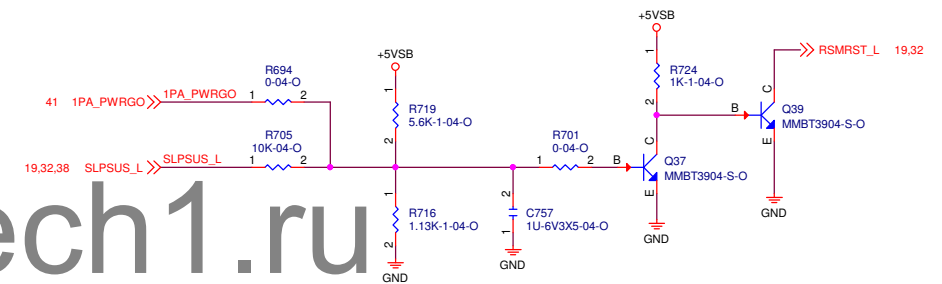
## VCCIO & VR ENABLE



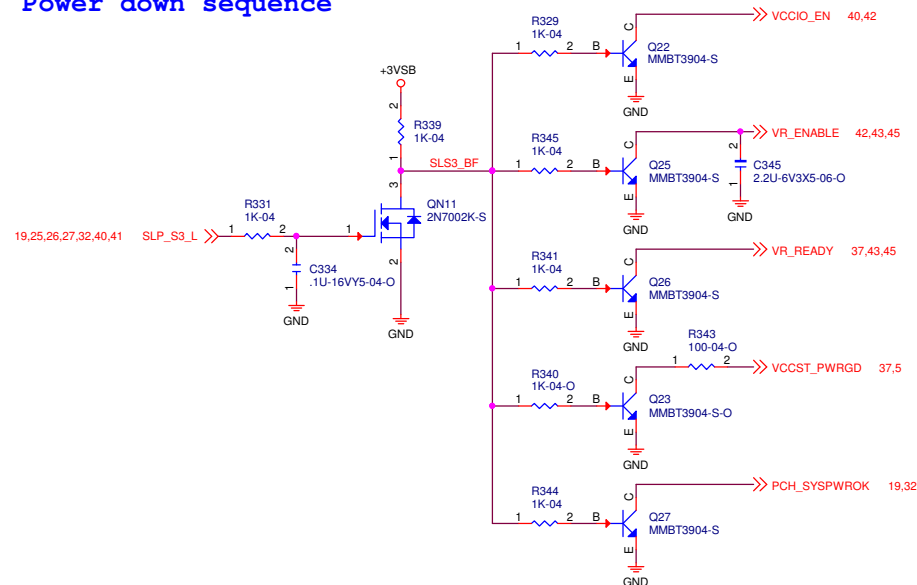
## PCH\_PWROK & VCCST



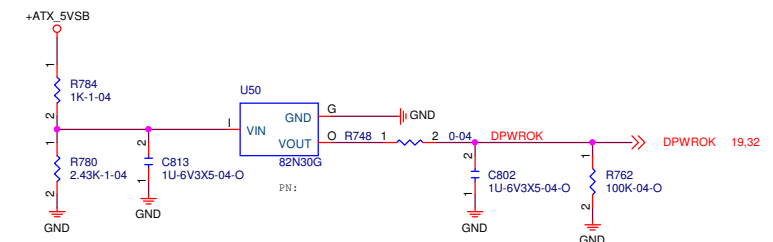
## RSMRST#

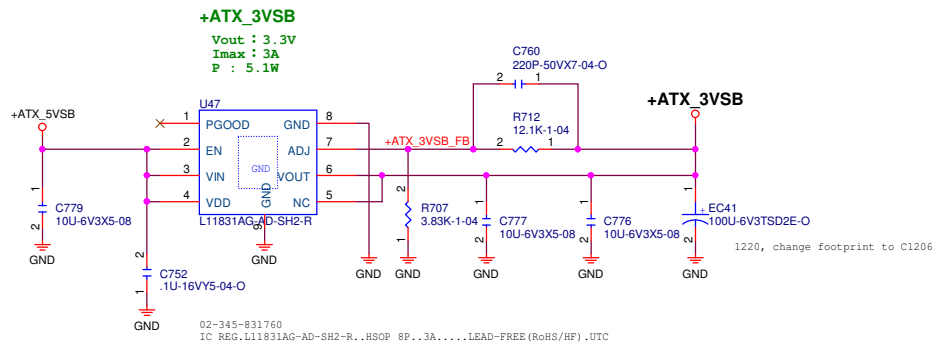
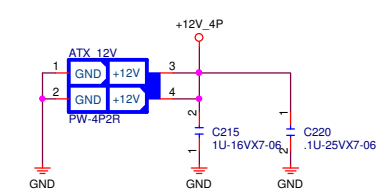
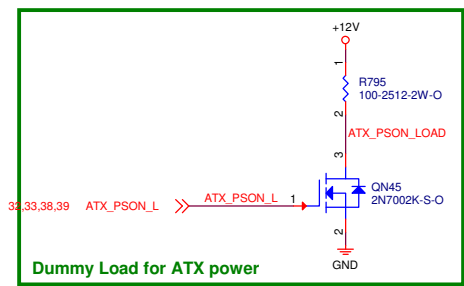
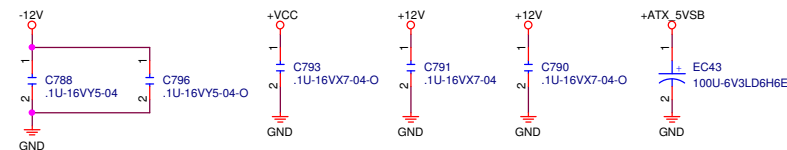
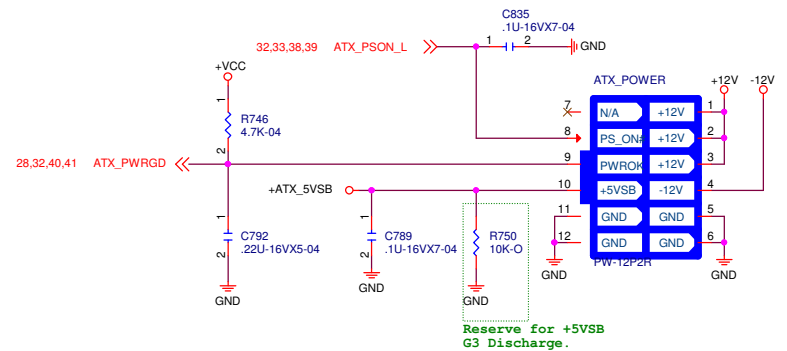


## Power down sequence



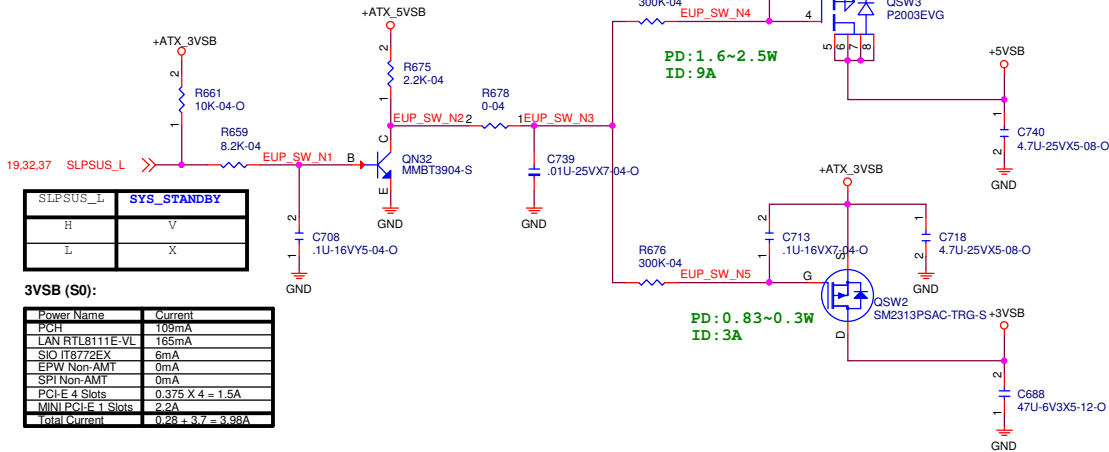
## DPWROK





# www.aitech1.ru

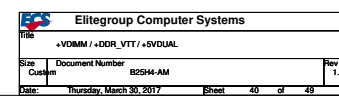
## EuP Lot6 Power Saving Circuit



SLPSUS_L	SYS_STANDBY
H	V
L	X

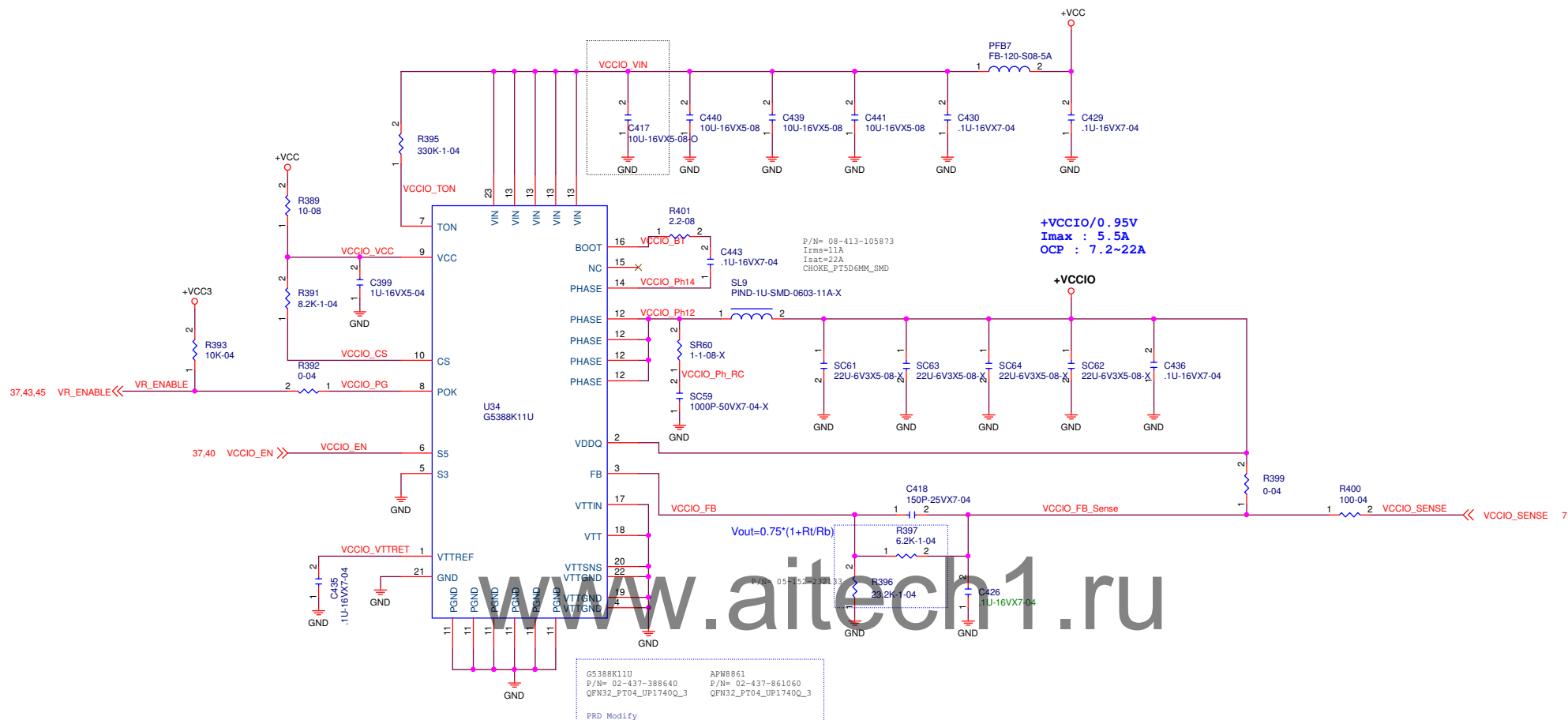
Power Name	Current
PCH	109mA
LAN RTL8111E-VL	165mA
SIO I16772EX	6mA
EPW Non-AMT	0mA
SPI Non-AMT	0mA
PCI-E 4 Slots	0.375 X 4 = 1.5A
MINI PCI-E 1 Slots	2.2A
Total Current	0.28 + 3.7 = 3.98A









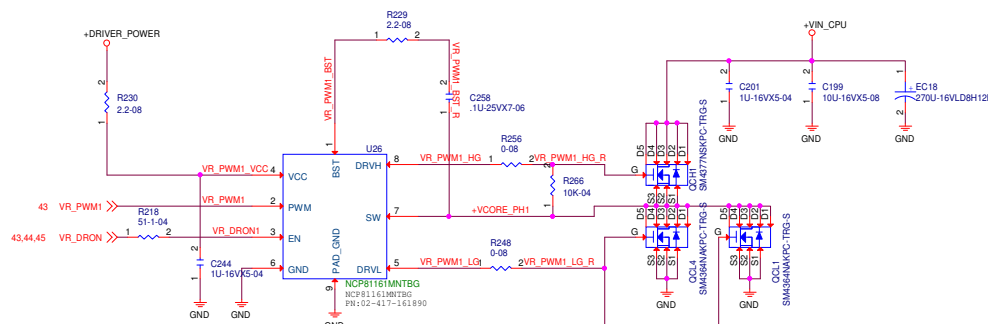
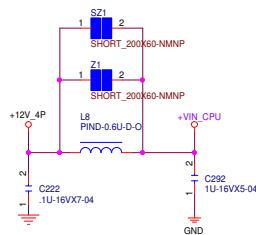
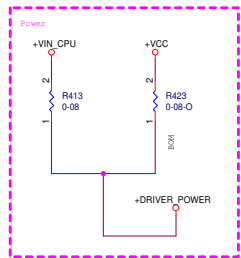




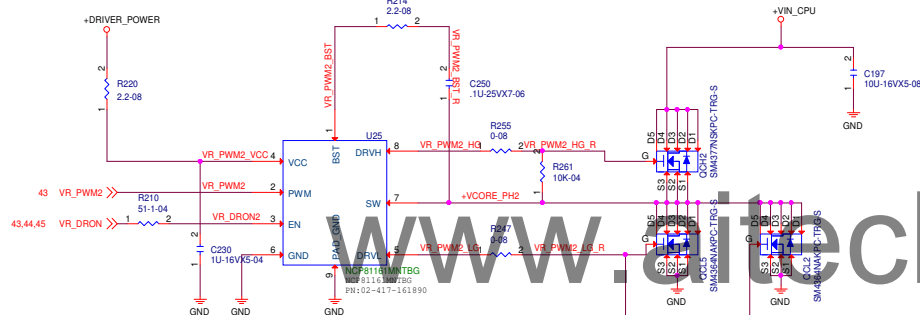
SKL-S VCCVID 0.55~1.5V  
42 65W 35W  
TDC 61A 53A  
IMAX 79A 66A

Imax : 79A  
94.8~118.5A ( Vendor Check)

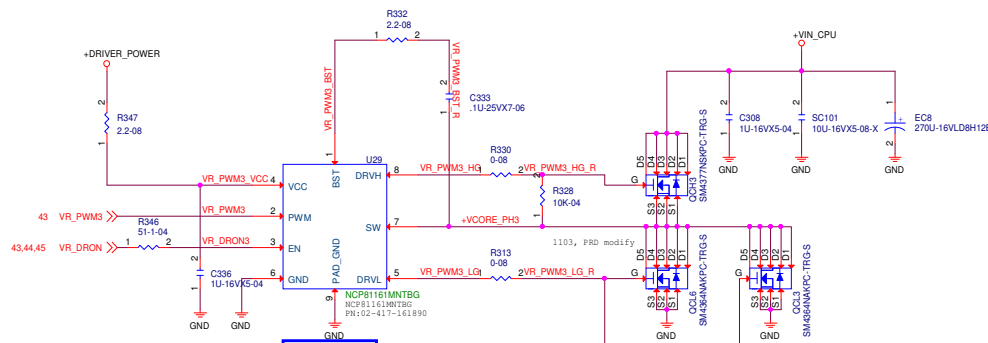
Vin = 12V  
Fs = 340khz  
Iout = 79A  
Vin Irms = 8.23A  
MLCC ripple current = 3A  
LIR = 37.2%  
Cin\_cap = 270uF\*3, 4.7uF\*3  
Cout\_cap = 560uF\*5  
OCP = 94.8~118.5A



BOTTOM PAD  
CONNECT TO  
GND Through  
4 VIAs



BOTTOM PAD  
CONNECT TO  
GND Through  
4 VIAs



BOTTOM PAD  
CONNECT TO  
GND Through  
4 VIAs

